```
     CAS/STN FILE 'WPIX' ENTERED AT 15:10:13 ON 09 AUG 2004
L1        47747   S    H01L023/ICM
L2            1   S    L1 AND INTERPOS?(3A)(MU OR MUM OR MICRON)
L3          193   S    L1 AND INTERPOS?(4A)(DIELEC###### OR INSULAT########)
L4           76   S    L1 AND INTERPOS?(4A)(RESIN OR EPOX####### OR POLYMER#######)
L5           15   S    L3 AND L4
L6           15   S    L5 NOT L2
L7           16   S    L2 OR L6
L8               SEL PLU=ON  L7 1- ICM :       16 TERMS
L9               SEL PLU=ON  L7 1- MC :       45 TERMS

     FILE 'HCAPLUS' ENTERED AT 15:41:50 ON 09 AUG 2004
L10         148   S    (PCB OR PRINTED CIRCUIT BOARD)(W)RESIN
L11              SEL PLU=ON  L10 1- RN :      475 TERMS
L12     4109118   S    L11
L13      107449   S    L12(L)RESIN
L14          98   S    L10 AND L13

     FILE 'REGISTRY' ENTERED AT 15:44:50 ON 09 AUG 2004
L15         475   S    L11
L16         346   S    L15 AND C/ELS

     FILE 'HCAPLUS' ENTERED AT 15:45:15 ON 09 AUG 2004
L17       87982   S    L16(L)RESIN
L18        5426   S    EPOX####### AND IMID######
L19         394   S    BISMAL######## AND TRIAZINE
L20       12350   S    POLYMID? OR (IMID## AND (POLY OR POLYMER OR HOMOPOLYMER OR RESIN))

     FILE 'REGISTRY' ENTERED AT 15:48:02 ON 09 AUG 2004
L21        1679   S    EPOX####### AND IMID######
L22        7720   S    POLYMID? OR (IMID## AND (POLY OR POLYMER OR HOMOPOLYMER OR RESIN))
L23          67   S    KAPTON
L24          32   S    UPILEX
L25           0   S    PCB RESIN
L26           0   S    PCB AND RESIN
L27          35   S    FR4 OR FR 4
L28        2258   S    CYANATE AND (ESTER OR POLYESTER)
L29         116   S    (POLYESTER/PCT OR "POLYESTER FORMED"/PCT) AND CYANATE

     FILE 'HCAPLUS' ENTERED AT 15:53:24 ON 09 AUG 2004
L30        1063   S    INTERPOS######## AND (L16 OR L10 OR (L17 OR L18 OR L19 OR L20) OR (L21 OR L22 OR L23 OR
L24 OR L25 OR L26 OR L27 OR L28 OR L29) OR BT EPOXY OR BT(2A)RESIN OR BISMAL######(2A) TRIAZ###### OR
BISMALEIMIDETRIAZIN#### OR BISMALEIMIDOTRIAZIN#####)
L31          30   S    L30 AND THIN FILM
L32           3   S    L30 AND (ULTRA THIN OR ULTRATHIN)
L33          36   S    L30 AND (THICK###### OR THIN)(3A)INTERPOS##########
L34         450   S    L30 AND (MU OR MICRON OR MUM OR MICROMET##### OR NM OR NANOMET##### OR ANG OR ANGSTROM OR
MONOLAYER#### OR 10 OR 20 OR 30 OR 35 OR 40 OR 45 OR 50 OR 55 OR 60 OR 65 OR 70 OR 75 OR 80 OR 85 OR 90 OR 95 OR
100)
L35          85   S    L30 AND (MU OR MICRON OR MUM OR MICROMET##### OR NM OR NANOMET##### OR ANG OR ANGSTROM OR
MONOLAYER#### OR 10 OR 20 OR 30 OR 35 OR 40 OR 45 OR 50 OR 55 OR 60 OR 65 OR 70 OR 75 OR 80 OR 85 OR 90 OR 95 OR
100)(5A)(INTERPOS######## OR THICKNESS)
L36       14021   S    L8
L37           3   S    L36 AND (L31 OR L32 OR L33 OR L34 OR L35)

     FILE 'WPIX' ENTERED AT 15:59:12 ON 09 AUG 2004
L38              SEL PLU=ON  L7 1- IC :       29 TERMS

     FILE 'HCAPLUS' ENTERED AT 15:59:21 ON 09 AUG 2004
L39       41642   S    L38
L40          11   S    L39 AND (L31 OR L32 OR L33 OR L34 OR L35)
L41           8   S    L40 NOT L37
L42          93   S    RESIN####(2A)INTERPOS########
L43          12   S    (L31 OR L32 OR L33 OR L34 OR L35) AND L42
L44           9   S    L43 NOT L40
L45          10   S    MONOLAYER####(2A)INTERPOS########
L46           0   S    MONO LAYER####(2A)INTERPOS########
L47           1   S    (L31 OR L32 OR L33 OR L34 OR L35) AND L45
L48           9   S    L45 NOT  L47
L49              SEL PLU=ON  L48 1- RN :       77 TERMS

     FILE 'REGISTRY' ENTERED AT 16:03:21 ON 09 AUG 2004
L50          77   S    L49
L51          59   S    L50 AND C/ELS
L52           1   S    L51 AND (RESIN OR POLY OR POLYMER OR EPOX###### OR IMIDE OR HOMOPOLYMER OR COPOLYMER OR
MONOMER)
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```
     FILE 'HCAPLUS' ENTERED AT 16:04:26 ON 09 AUG 2004
L53           1   S    L48 AND L52
L54           8   S    L48 NOT L53
L55           2   S    L54 AND (THIN###### OR THICK######## OR
                  DIELEC####### OR INSULAT########)(3A)INTERPOS##########
L56           2   S    L51 AND L55
L57        4301   S    "ULTRATHIN FILMS"/CT
L58           0   S    (L31 OR L32 OR L33 OR L34 OR L35) AND L57
L59           6   S    L57 AND INTERPOS#########
L60           0   S    (L21 OR L22 OR L23 OR L24 OR L25 OR L26 OR L27 OR L28 OR L29) AND L59
L61             SEL PLU=ON  L59 1- RN :      23 TERMS

     FILE 'REGISTRY' ENTERED AT 16:08:48 ON 09 AUG 2004
L62          23   S    L61
L63           3   S    L62 AND C/ELS

     FILE 'HCAPLUS' ENTERED AT 16:09:04 ON 09 AUG 2004
L64           1   S    L59 AND L63
L65           6   S    L59 OR L64
L66        9425   S    (THIN OR ULTRATHIN)(4A)(SPACER OR INTERLAYER###### OR INTERVEN##### OR INTER OR BETWEEN)
L67         364   S    ((L17 OR L18 OR L19 OR L20) OR RESIN OR (L21 OR L22 OR L23 OR L24 OR L25 OR L26 OR L27 OR
L28 OR L29)) AND L66
L68       41642   S    L38
L69           7   S    L68 AND L67
L70           6   S    L67 AND (BGA OR LGA OR LANDGRID OR BALLGRID OR GRID ARRAY OR BUMP## OR BALL OR FLIP CHIP
OR FLIPCHIP)
```

09aug04 15:37:05 User259284 Session D2863.3

SYSTEM:OS - DIALOG OneSearch
File 34:SciSearch(R) Cited Ref Sci 1990-2004/Aug W1
(c) 2004 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info

Set	Items	Description
S1	1	CR='BEYER V, 1998, P112, P 3 INT CSP C BINGH'

10aug04 09:36:58 User259284 Session D2864.2

SYSTEM:OS - DIALOG OneSearch
File 348:EUROPEAN PATENTS 1978-2004/Aug W01
(c) European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040805,UT=20040729
(c) WIPO/Univentio

```
Set     Items   Description
S1        194   (MICRON?? OR MU OR MUM)(2N)INTERPOS??????????
S2       2583   (THICK???????? OR THIN?????? OR ULTRATHIN??????)(6N)INTERPOS??????????
S3        106   1AND2
S4      71466   (THICK???????? OR THIN?????? OR ULTRATHIN??????)(6N)(MICRON?? OR MU OR MUM)
S5        103   3AND4
S6         65   (AA OR ANG OR ANGS OR ANGSTROM?? OR NM)(2N)INTERPOS??????????
S7         40   2AND6
S8      24772   (THICK???????? OR THIN?????? OR ULTRATHIN??????)(6N)(AA OR ANG OR ANGS OR
ANGSTROM?? OR NM)
S9         40   7AND8
S10       143   S5 OR S9
S11      6218   (RESIN?? OR ORGANIC?? OR POLYMER???? OR PI OR IMIDE?? OR POLYIMID???? OR
INSULAT?????? OR DIELEC??????)(3N)INTERPOS??????????
S12        51   10AND11
S13         1   S12 AND (Z()AXIS OR VERTICAL??)(4W)CONDUCT???????
S14      2638   CONDUCT??????(4W)(Z()AXIS OR VERTICAL??)(4W)CONDUCT???????
S15         0   12AND14
S16     18619   (Z OR VERTICAL??)(8N)(CONDUCT??????? OR ELECTRIC????)
S17         1   12AND16
S18         1   S13 OR S17
S19        13   S12 AND IC=H01L?
S20         1   (S1 OR S3 OR S5 OR S6 OR S9:S10 OR S12 OR S19) AND (MONOLA-
              YER???? OR MONOMOLEC??????? OR MONO)(6N)INTERPOS???????????
S21         0   S20 NOT S18
S22         0   1AND3AND4AND6AND9AND10AND12
S23         0   S12 AND (FLIP??????? OR BGA?? OR LGA?? OR BALL??????? OR GRID????()ARRAY????)/TI,AB
S24         3   S12 AND (FLIP??????? OR BGA?? OR LGA?? OR BALL??????? OR GRID????()ARRAY????)
S25        14   S19 OR S24
S26        14   S25 NOT S20
S27         5   INTERPOS??????(3W)(MU OR MICRON?? OR AA OR ANG OR ANGS OR ANGSTROM?? OR NM OR
NANOMETER??)(W)THICK????????
S28        36   (MU OR MICRON?? OR AA OR ANG OR ANGS OR ANGSTROM?? OR NM OR NANOMETER??)(W)
THICK????????(3W)INTERPOS????????
S29         7   S26 AND S27:S28
S30        39   (S1:S3 OR S5:S7 OR S9:S13) AND S27:S28
S31      2459   (RESIN?? OR POLYMER????? OR PLASTIC??? OR ORGANIC?? OR IMI-
              DO?? OR IMIDE?? OR POLYIMID?????)(3N)INTERPOS????????
S32         3   30AND31
```

09aug04 15:14:10 User259284 Session D2863.2

File 2:INSPEC 1969-2004/Aug W1 (c) Institution of Electrical Engineers

Set	Items	Description
S1	27	INTERPOS????????? AND (ULTRATHIN OR ULTRA()THIN OR MONOLAYER??????)
S2	141	INTERPOS???????? AND (PLASTIC?? OR POLYMER?? OR HOMOPOLYMER???? OR MONOMER???? OR RESIN???? OR POLYIMID? OR IMIDE??)
S3	333	INTERPOS?????????(4N)(THICK??????? OR THIN?? OR FILM?? OR LAYER???)
S4	7	1AND2
S5	41	2AND3
S6	60	S1:S3 AND (FLIPCHIP? OR FLIP()CHIP???? OR FC OR FCP? ? OR BGA? ? OR LGA? ? OR LANDGRID????? OR BALLGRID????? OR GRID????(2N)ARRAY?????)
S7	38	S1:S3 AND BALL???????(2N)ARRAY?????
S8	26	S1:S3 AND BUMP??
S9	9	S1:S3 AND (VERTICAL???? OR Z)
S10	14	1AND3
S11	13	(S4:S5 OR S10) AND S6
S12	7	(S4:S5 OR S10) AND S7
S13	6	(S4:S5 OR S10) AND S8
S14	3	(S4:S5 OR S10) AND S9
S15	0	7AND8AND9
S16	10	7AND8
S17	0	7AND9
S18	0	8AND9
S19	3	1AND2AND3
S20	5	S1:S3 AND INTERPOS???????(4N)RESIN??
S21	38	6AND7
S22	17	6AND8
S23	10	7AND8
S24	2	10AND11
S25	397	INTERPOS?????????/TI,DE,ID
S26	140	S1:S24 AND S25
S27	63	(S1 OR S4:S24) AND S25
S28	47	6AND27
S29	18	(S4 OR S5 OR S10) AND S27
S30	10	(S4 OR S5 OR S10) AND S28 AND S29
S31	6	INTERPOS?????????(4N)(ULTRA OR MONOLAYER??????)
S32	40	S4 OR S9 OR S12:S20 OR S23 OR S24 OR S30:S31
S33	16	S32 AND (PITCH?????? OR SPAC??????? OR CENTER??????? OR PADS OR ACTIVE OR PASSIVE)
S34	20	S32 AND NI=?
S35	12	S34 NOT S33
S36	12	S32 NOT (S34 OR S33)
S37	38	AU=RAO V?
S38	723	AU=RAO, V?
S39	2	S37:S38 AND INTERPOS???????????
S40	0	AU=HOWELL W?
S41	38	AU=HOWELL, W?
S42	1	S41 AND INTERPOS???????????
S43	50	S1:S36 AND CS=IBM
S44	38	S43 AND INTERPOS?????????/TI,DE,ID
S45	35	S44 NOT (S39 OR S36 OR S35 OR S33)
S46	0	S45 AND RESIN????
S47	1	S45 AND (INSULAT??????? OR DIELEC???????)(6N)INTERPOS????????
S48	54	(INSULAT??????? OR DIELEC???????)(6N)INTERPOS????????
S49	52	S48 NOT (S47 OR S39 OR S36 OR S35 OR S33)
S50	6	S49/2001-2004
S51	46	S49 NOT S50
S52	0	S51 AND FLIP???????????
S53	0	S51 AND BGA
S54	0	S51 AND (BALL????? OR BUMP??????)
S55	1	S51 AND INTERPOS???????????/TI
S56	119	INTERPOS?????????/TI
S57	9	S56/1999
S58	14	S56/2000
S59	7	S56/1998
S60	13	S36 OR S39 OR S47
S61	30	S57:S59 NOT (S47 OR S39 OR S36 OR S35 OR S33 OR S60)
S62	3	S61 AND FLIP????????
S63	1	S61 AND (BGA OR LGA OR GRID?????)
S64	3	S61 AND (BGA OR LGA OR GRID????? OR BALL?????? OR BUMP????????)
S65	4	S62:S64
S66	2	S61 AND (IMID?? OR POLYIMID?????)
S67	1	S66 NOT S65

```
     FILE 'REGISTRY' ENTERED AT 12:18:18 ON 10 AUG 2004
L1            67   S    KAPTON
L2            32   S    UPILEX
L3            35   S    FR4 OR FR 4
L4            84   S    CYANATE ESTER

     FILE 'HCAPLUS' ENTERED AT 12:19:26 ON 10 AUG 2004
L5          2608   S    L1(L)(THIN OR ULTRATHIN OR LAYER OR FILM OR INTERL####### OR INTERPOS#######)
L6          2720   S    L2(L)(THIN OR ULTRATHIN OR LAYER OR FILM OR INTERL####### OR INTERPOS#######)
L7            73   S    L3(L)(THIN OR ULTRATHIN OR LAYER OR FILM OR INTERL####### OR INTERPOS#######)
L8             2   S    L4(L)(THIN OR ULTRATHIN OR LAYER OR FILM OR INTERL####### OR INTERPOS#######)
L9             0   S    L4 AND (SEMICOND######### OR H01L?/IC)
L10           80   S    CYANATE ESTER AND (SEMICOND######### OR H01L?/IC)
L11          217   S    L5 AND (SEMICOND######### OR H01L?/IC)
L12          292   S    L6 AND (SEMICOND######### OR H01L?/IC)
L13            2   S    L7 AND (SEMICOND######### OR H01L?/IC)

     FILE 'REGISTRY' ENTERED AT 12:22:40 ON 10 AUG 2004
L14            1   S    33294-14-3
L16            1   S    GOLD/CN

     FILE 'HCAPLUS' ENTERED AT 12:25:00 ON 10 AUG 2004
L17       141109   S    L16
L18           15   S    L10 AND (FLIP CHIP OR FLIPCHIP OR BGA OR BALL GRID OR GRID ARRAY OR BALLGRID OR LGA OR
LANDGRID OR LAND GRID OR (AU OR GOLD)(2A)BUMP OR L17 )

     FILE 'REGISTRY' ENTERED AT 12:25:25 ON 10 AUG 2004
L19            1   S    GOLD/CN

     FILE 'HCAPLUS' ENTERED AT 12:25:26 ON 10 AUG 2004
L20       141109   S    L19
L21           13   S    L11 AND (FLIP CHIP OR FLIPCHIP OR BGA OR BALL GRID OR GRID ARRAY OR BALLGRID OR LGA OR
LANDGRID OR LAND GRID OR (AU OR GOLD)(2A)BUMP OR L20 )

     FILE 'REGISTRY' ENTERED AT 12:25:37 ON 10 AUG 2004
L22            1   S    GOLD/CN

     FILE 'HCAPLUS' ENTERED AT 12:25:37 ON 10 AUG 2004
L23       141109   S    L22
L24           15   S    L12 AND (FLIP CHIP OR FLIPCHIP OR BGA OR BALL GRID OR GRID ARRAY OR BALLGRID OR LGA OR
LANDGRID OR LAND GRID OR (AU OR GOLD)(2A)BUMP OR L23 )
L25            0   S    INTERPOS######## AND L18
L26            2   S    INTERPOS######## AND L21
L27            2   S    INTERPOS######## AND L24
L28            2   S    L26 AND L27
L29            0   S    L7 AND ULTRATHIN
L30            1   S    L7 AND ULTRA THIN
L31            1   S    L7 AND THIN FILM
L32            2   S    (L30 OR L31)
L33           70   S    L7 AND (LAYER###### OR FILM## OR INTERPOS########)
L34            2   S    L7 AND INTERPOS########

     FILE 'REGISTRY' ENTERED AT 12:30:58 ON 10 AUG 2004
L35            1   S    33294-14-3

     FILE 'HCAPLUS' ENTERED AT 12:34:58 ON 10 AUG 2004
L36            2   S    PCB RESIN
L37         1185   S    PCB AND (CIRCUIT BOARD OR PRINTED CIRCUIT###)
L38          161   S    RESIN/TI,IT,ST AND L37
L39         5048   S    RESIN(3A)(PCB OR CIRCUIT BOARD OR PRINTED CIRCUIT###)
L40           72   S    L37 AND L39
L41          167   S    L38 OR L40
L42            2   S    L41 AND INTERPOS#########
L43              SEL PLU=ON  L42 1- RN :       2 TERMS

     FILE 'REGISTRY' ENTERED AT 12:38:07 ON 10 AUG 2004
L44            2   S    L43

     FILE 'HCAPLUS' ENTERED AT 12:38:30 ON 10 AUG 2004
L45            3   S    L41 AND (ULTRA THIN OR ULTRATHIN OR THIN FILM)
L46              SEL PLU=ON  L45 1- RN :       7 TERMS

     FILE 'REGISTRY' ENTERED AT 12:39:41 ON 10 AUG 2004
L47            7   S    L46
L48            1   S    L47 AND C/ELS

     FILE 'HCAPLUS' ENTERED AT 12:39:57 ON 10 AUG 2004
L49            1   S    L45 AND L48
L50            3   S    L45 OR L49
```

STIC Search Results Feedback Form

EIC 2800

Questions about the scope or the results of the search? Contact ***the EIC searcher or contact*:**

Jeff Harrison, EIC 2800 Team Leader
571-272-2511, JEF 4B68

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 2810*
- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
  (journal articles, conference proceedings, new product announcements etc.)

- *Relevant prior art **not found**:*
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2800, CP4-9C18

26/3,AB,K/11 (Item 11 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00361907
Switching element
PATENT ASSIGNEE: CANON KABUSHIKI KAISHA, (542366), 3-30-2 Shimomaruko, Ohta-ku, Tokyo,
INVENTOR: Sakai, Kunihiro, 43-12-301, Higashinaruse, Isehara-shi Kanagawa-ken, (JP)
PATENT (CC, No, Kind, Date): EP 330395 A2 890830 (Basic)
EP 330395 A3 900530
EP 330395 B1 970507
PRIORITY (CC, No, Date): JP 8839829 880222
INTERNATIONAL PATENT CLASS: **H01L-031/08; H01L-031/02;** H03K-017/78

ABSTRACT EP 330395 A2
A switching element comprises two electrodes and an **insulating** or semiconductive region **interposed** between the two electrodes, and further comprises a photosensitive region having electrical characteristics which are changed by irradiation of light.

...SPECIFICATION may be used so long as it is sufficiently thin. The thickness is preferably 2000 A or less, more preferably 1000 A or less (1 **nm** = 10 A).
Thin organic films having semiconductivity or insulating properties are formed between the electrodes. These thin films can be formed by utilizing vapor deposition or molecular beam...

CLAIMS 1. A switching device comprising:
a switching element (11, 12, 11) comprising two electrodes (11) and an **organic insulative region (12) having a thickness not in excess of 100 nm interposed** between said two electrodes (11) said region (12) being in the form of material selected from the group consisting of molecules having a pi-electron...

...photosensitive region.
2. A switching device comprising:
a switching element (11, 12, 11) comprising two electrodes (11) and an organic insulative region (12) having a **thickness** not in excess of 100 **nm interposed** between said two electrodes (11) said region (12) being in the form of material selected from the group consisting of molecules having a pi-electron...

...device comprising:
a switching element (11, 12) comprising a first electrode (11) and monomolecular or accumulated films of an **organic insulative region (12) having a thickness not exceeding 100 nm** adjacent said first electrode (11) said region (12) being in the form of material selected from the group consisting of molecules having a pi-electron...

6. A switching device as claimed in claim 4 or 5, characterised in that the thickness of each of said organic **thin** films is 0.5 to 50 **nm**.

FAMILY MEMBER OF US 5,170,238

L13 ANSWER 2 OF 2 **HCAPLUS COPYRIGHT ACS on STN**
AN 1994:581462 HCAPLUS Full-text
DN 121:181462
ED Entered STN: 15 Oct 1994
TI Coverlet films for flexible printed circuit boards
IN Matsumoto, Satoshi; Kobayashi, Shoji
PA Toray Industries, Japan

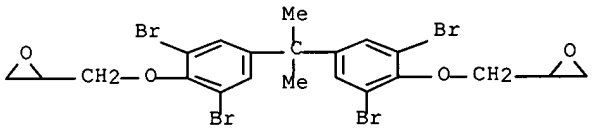
PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 06041502	**A2**	**19940215**	**JP 1992-196927**	**19920723**
PRAI JP 1992-196927		**19920723**		

AB The title films, with good punching effects, suitable adhesion strength and releasing property of adhesive, and good storage stability because of not using releasing agent, comprise a base film (e.g., 25-μm Kapton 100H film), an adhesive layer (e.g., a blend of 75% nylon 6-nylon 66-nylon 610-nylon 12 copolymer, 25% Epikote 834, 5 phr 4,4'- diaminodiphenylsulfone, and 2 phr Sumilite 50087), and a protective sheet containing a stretched polypropylene layer on the adhesive side and a PET layer.

IT Epoxy resins, uses
IT **33294-14-3**, Epikote 5050
(adhesives containing, for coverlet **films** with PET-polypropylene laminated protecting **layers**, for flexible printed circuit boards)
RN 33294-14-3 HCAPLUS
CN Oxirane, 2,2'-[(1-methylethylidene)bis[(2,6-dibromo-4,1-phenylene)oxymethylene]]bis-, homopolymer (9CI) (CA INDEX NAME)

CM 1

CRN 3072-84-2
CMF C21 H20 Br4 O4



26/3,AB,K/14 (Item 14 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00254306
High performance integrated circuit packaging structure.
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road,
INVENTOR:
Jacobs, Scott Laurence, 14602 Barkwood Court, Chester Virginia 23831,
PATENT (CC, No, Kind, Date): EP 267360 A2 880518 (Basic)
EP 267360 A3 881109
EP 267360 B1 920826
PRIORITY (CC, No, Date): US 929946 861112
INTERNATIONAL PATENT CLASS: **H01L-023/52**

ABSTRACT EP 267360 A2
A high speed, high performance integrated circuit packaging structure that may be used for emulating wafer scale integration structures. The preferred embodiment comprises an interposer (9) having a base substrate having alternating insulation and conductive layers thereon, wherein a plurality of the conductive layers are wiring means which are adapted for maintaining an extremely low noise level in the package. The low noise level and low resistance and capacitance of the wiring means allows a plurality of discrete semiconductor segments (32) to be mounted on and interconnected by the integrated circuit package with a significantly reduced number of drivers and receivers than required by Rent's Rule. Each integrated circuit structure (9) of the present invention emulates a large chip or wafer scale integration structure in performance without having to yield the large chip or wafer, and without redundancy schemes. A plurality of these integrated circuit packaging structures (9) are combined by decals (29, 31) to form a central processing unit (1) of a computer or a portion thereof. In an alternate preferred embodiment, the base substrate of the interposer is made of silicon and any required drivers are formed therein, thus substantially eliminating the need for any drivers on each of the discrete semiconductor segments (32).

...SPECIFICATION

These wiring layers may be of any conductive material, preferably copper. The **insulation** 44 between and around the conductive lines is preferably **material of a low dielectric constant, most preferably polyimide.**

The solder **balls** must be small so that the impedance between the internal circuits on the semiconductor segments 32 and the wiring of interposer is substantially constant, allowing the internal circuit groups to communicate on the interposer with substantially no drivers and receivers. In preferred form, solder **balls** 34 are 25-75 micrometer (1-3 mils) in diameter. In this size range, the solder joints electrically resemble a thin film stud or metal...required to operate without the majority of drivers and receivers, these wiring structures are readily manufacturable, and result in high yields.

Family member of US 4,811,082

26/3,AB,K/9 (Item 9 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) European Patent Office. All rts. reserv.
00379753
Bipolar power semiconductor device and process for its manufacture.
PATENT ASSIGNEE:
SGS-THOMSON MICROELECTRONICS S.r.l., (1014061), 50 Stradale Primosole,
INVENTOR:
Oliveri, Carmelo, 11 Via Mongibello, Frazione Rovittello, I-95030
Patti, Alfonso, 11 Via Rosso di San Secondo, I-95100 Catania CT, (IT)
Fleres, Sergio, 46 Via E. d'Angio, I-95125 Catania CT, (IT)
PATENT (CC, No, Kind, Date): EP 341221 A2 891108 (Basic)
EP 341221 A3 900822
EP 341221 B1 940803
PRIORITY (CC, No, Date): IT 886611 880505
INTERNATIONAL PATENT CLASS: **H01L-029/08; H01L-029/73**

ABSTRACT EP 341221 A2
A bipolar power semiconductor device, particularly a transistor, of structure formed by a matrix array of cells operating as emitter regions, comprises two separated and superposed layers of metal, one for the base and one for the emitter, separated by a layer of polyimide, as an intermediate dielectric (figure 3).

...SPECIFICATION order to solve this problem, according to the present invention, the two metallizations are superposed vertically, and **between the two layers** of metal **an intermediate dielectric layer is interposed**. It is thus possible to realize a structure in which the emitter is formed by a set of single cells, spread out on the base...
layer 6 on the oxide of about 20(mu) in a radial direction.
Again as a non-limitative example, the first metallization can have a thickness of around 3(mu) and the second metallization can have a thickness of 6(mu),
while the **interposed polyimide layer can have a thickness of from about 3 to 3,6(mu)**. The process by which the silicon/metal contacts are obtained in the process according to the invention...

FAMILY member of US 5,032,887

36/9/12
DIALOG(R) File 2: INSPEC

01558113 INSPEC Abstract Number: A80080402, B80039712
Title: Conduction in MIM structures with an organic monomolecular layer at high electric fields
Author(s): Furtlehner, J.-P.; Messier, J.
Author Affiliation: SES/LERA, CENS, Gif-sur-Yvette, France
Journal: Thin Solid Films vol.68, no.1 p.233-9
Publication Date: 1 May 1980 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
Language: English Document Type: Journal Paper (JP)
Treatment: Experimental (X)
Abstract: The influence of **one organic monolayer (30 AA thick)** on the electronic conduction through Al/Al/sub 2/O/sub 3//Al structures at very high DC electric fields (E>10/sup 6/ V cm/sup -1/) between 20 and 120 degrees C was studied. One **interposed monolayer** reduces the injected current from aluminium into alumina by a factor of 100-1000. This reduction in the conduction current cannot be explained by one single potential barrier associated with the organic layer. It is necessary to take into account the presence of a natural oxide layer on the counterelectrode and the trapping of electrons in the organic layer or at the interface. (11 Refs)

L28 ANSWER 2 OF 2 **HCAPLUS COPYRIGHT ACS on STN**
AN 2001:851773 HCAPLUS Full-text
DN 135:379722
ED Entered STN: 23 Nov 2001
TI Wafer-scale assembly of chip-size packages
IN Heinen, Katherine G.; Edwards, Darvin R.; Jacobs, Elizabeth G.
PA Texas Instruments Inc., USA

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001044197	A1	20011122	US 1998-186973	19981105
	US 6730541	B2	20040504		
	EP 918354	A2	19990526	EP 1998-203878	19981120
	EP 918354	A3	20000510		
PRAI	**US 1997-66256P**	**A**	**19971120**		

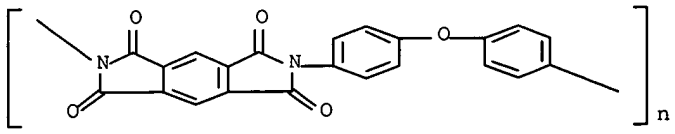
AB A wafer-scale assembly apparatus for integrated circuits and a method for forming the wafer-scale assembly are disclosed. A **semiconductor** wafer including a plurality of circuits is provided with a plurality of metal contact pads as elec. entry and exit ports. A 1st wafer-scale patterned polymer film carrying solder balls for each of the contact pads on the wafer is positioned opposite the wafer and the film are aligned. The film is brought into contact with the wafer. Radiant energy in the near IR spectrum is applied to the backside of the wafer, heating the wafer uniformly and rapidly without moving the **semiconductor** wafer. Thermal energy is transferred through the wafer to the surface of the wafer and into the solder balls, which reflow onto the contact pads, while the thermal stretching of the polymer film is mech. compensated. The uniformity of the height of the liquid solder balls is controlled either by mech. stoppers or by the precision linear motion of motors. After cooling, the solder balls solidify and the 1st polymer film is removed. The process is repeated for assembling sequentially a wafer-scale patterned **interposer** overlying all of the solder balls and the wafer and contacting each solder ball with a soldered joint, and a 2nd wafer-scale patterned film carrying solder balls contacting the **interposer**. In each process, the wafer is heated uniformly and rapidly and without moving it, the alignment is maintained during heating by mech. compensating for the thermal stretching of the polymer film, and the uniformity of the height of the liquid solder balls is controlled by mech. stoppers or position closed-loop linear actuators. The 2nd film is removed after cooling. Other embodiments are also disclosed.

IT Solders
(balls; wafer-scale assembly of chip-size packages)

IT Polyimides, uses
RL: DEV (Device component use); USES (Uses)
(insulating **interposer**; wafer-scale assembly of chip-size packages)

IT **25036-53-7, Kapton**
(**film**, insulating **interposer**; wafer-scale assembly of chip-size packages)

RN 25036-53-7 HCAPLUS
CN Poly[(5,7-dihydro-1,3,5,7-tetraoxobenzo[1,2-c:4,5-c']dipyrrole-2,6(1H,3H)-diyl)-1,4-phenyleneoxy-1,4-phenylene] (9CI) (CA INDEX NAME)



IT **7440-57-5**, Gold, uses
(metal contact pads; wafer-scale assembly of chip-size packages)

RN 7440-57-5 HCAPLUS
CN Gold (8CI, 9CI) (CA INDEX NAME)

Au

L50 ANSWER 2 OF 3 **HCAPLUS COPYRIGHT ACS on STN**
AN 2001:338919 HCAPLUS Full-text
DN 134:335454
ED Entered STN: 11 May 2001
TI Method fabricating a laminated **printed circuit board**
IN Beyne, Eric; Lechleiter, Francois
PA Interuniversitair Microelektronica Centrum (IMEC), Belg.; Cimulec

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2001033925	A1	20010510	WO 2000-IB1725	20001106
	EP 1226743	A1	20020731	EP 2000-974728	20001106
	JP 2003513456	T2	20030408	JP 2001-534941	20001106
	US 6711813	**B1**	**20040330**	**US 2000-707311**	**20001106**
PRAI	**US 1999-163666P**	**P**	**19991105**		
	WO 2000-IB1725	W	20001106		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
WO 2001033925	ICM	H05K003-46

AB Method and apparatus of fabricating a core laminate **Printed Circuit Board** structure with highly planar external surfaces is provided. A pre-formed flat material including a 1st resinous sub-material and a 2nd carrier sub-material is used to planarize external surfaces. During lamination, uniform pressure is applied to the pre-formed flat sheet which covers the upper surface of the **printed circuit**. The resinous material of the 1st sub-material flows to fill the crevices, vias, etc. of the upper surface of the **PCB**. Also, due to the uniform pressure on the pre-formed flat sheet, the resinous 1st sub-material is planarized. This planarized surface provides a suitable base substrate for a **thin film** multilayer build-up structure and that provides elec. connections between the **thin film** top layers and the **Printed Circuit Board** - style core layers.

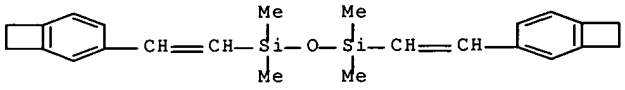
IT **124221-30-3**, Cyclotene
(dielec. layer; method fabricating a laminated **printed circuit board**)

RN 124221-30-3 HCAPLUS

CN Disiloxane, 1,3-bis(2-bicyclo[4.2.0]octa-1,3,5-trien-3-ylethenyl)-1,1,3,3-tetramethyl-, homopolymer (9CI) (CA INDEX NAME)

CM 1

CRN 117732-87-3
CMF C24 H30 O Si2

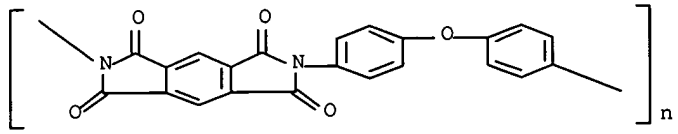


L28 ANSWER 1 OF 2 **HCAPLUS COPYRIGHT ACS on STN**
AN 2003:817845 HCAPLUS Full-text
DN 139:300252
ED Entered STN: 17 Oct 2003
TI **Dielectric interposer** for chip to substrate soldering
IN Brofman, Peter J.; Farooq, Shaji; Knickerbocker, John U.; Langenthal, Scott I.; Ray, Sudipta K.; Stalter, Kathleen A.
PA International Business Machines Corporation, USA
IC ICM **H01L023-48**

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003193093	A1	20031016	US 2003-427459	20030501
	US 6657313	B1	20031202	US 1999-233385	19990119
PRAI	**US 1999-233385**	**A3**	**19990119**		

AB A method of and device for preventing short circuits between solder joints in **flip chip** packaging. The dielec. interposer of the present invention has a plurality of apertures or vias which correspond to the I/O pads on a chip and substrate. Preferably, the **interposer** comprises a polyester film, glass, alumina, **polyimide**, a heat curable polymer or an inorg. powder filler in an organic material. More preferably, the interposer contains an adhesive or has adhesive layers disposed on the linear surfaces of the interposer. Cone shaped solder elements are formed within the apertures of the interposer. The dielec. interposer is positioned between a chip and substrate in an electronic module and thermally re-flowed to create an elec. and mech. interconnection. The interposer prohibits contact between the solder joints by isolating each of the joints and corresponding bonding pads. The interposer also prevents over compression of the solder joints by acting as a stand off.

IT Electric insulators
(**interposer**; dielec. **interposer** for chip to substrate soldering)
IT **25036-53-7, Kapton**
(dielec. **interposer** for chip to substrate soldering)
RN 25036-53-7 HCAPLUS
CN Poly[(5,7-dihydro-1,3,5,7-tetraoxobenzo[1,2-c:4,5-c']dipyrrole-2,6(1H,3H)-diyl)-1,4-phenyleneoxy-1,4-phenylene] (9CI) (CA INDEX NAME)



L6 **ANSWER** 2 OF 15 **WPIX COPYRIGHT THOMSON DERWENT on STN**
AN 2004-200263 [19] WPIX Full-text
CR 2004-059427 [06]
DNN N2004-158892 DNC C2004-079270
TI Flip chip electronic module intermediate product comprises **dielectric interposer** between chip and substrate and having apertures where conical solder elements are deposited.
DC A85 L03 U11
IN BROFMAN, P J; FAROON, S; KNICKERBOCKER, J U; LANGENTHAL, S I; RAY, S K; STALTER, K A
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6657313 B1 20031202 (200419)* 7 H01L023-48 <--
ADT US 6657313 B1 US 1999-233385 19990119
PRAI US 1999-233385 19990119
IC ICM **H01L023-48**
AB US 6657313 B UPAB: 20040318
NOVELTY - Flip chip electronic module intermediate product comprises a semiconductor chip (12, 42), a substrate (40) for mounting the chip, and a **dielectric interposer** (630) between the chip and the substrate and having apertures traversing its thickness.

Conical solder elements (637) are deposited within the apertures. The interposer separates the solder elements so that the solder elements are not in contact with an adjacent solder element.

USE - For electronic module.

ADVANTAGE - The assembly prevents short circuits between solder joints in flip chip packaging. This results in increased yield and reliability of resulting electronic module.

DESCRIPTION OF DRAWING(S) - The figures are elevational cross-sectional views of an electronic module and an interposer.

Semiconductor chips 12, 42
Substrate 40
Dielectric interposer 630
Adhesive layers 635
Conical solder elements 637
Dwg.5, 6/6
TECH US 6657313 B1 UPTX: 20040318
TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The solder elements are coated with tin. They are coated with lower melting temperature solder than the solder elements. The **dielectric interposer** further includes adhesive layers (635) disposed on linear surfaces of the interposer.

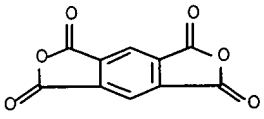
TECHNOLOGY FOCUS - **POLYMERS** - Preferred Materials: The **dielectric interposer** comprises polyester film, glass, alumina, **polyimide**, inorganic filler in organic polymer, heat curable polymer, or polymer containing an adhesive.

L37 **ANSWER** 3 OF 3 **HCAPLUS COPYRIGHT ACS on STN**
AN 2001:10763 HCAPLUS Full-text
DN 134:79732
ED Entered STN: 05 Jan 2001
TI Multilayer circuit boards free from breakage due to thermal fatigue
IN Kurita, Hideyuki; Nakamura, Masayuki
PA Sony Chemicals Corp., Japan
SO Eur. Pat. Appl., 11 pp.
CODEN: EPXXDW
DT Patent
LA English
IC ICM **H01L023-14**
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 38, 75
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1065717	A2	20010103	EP 2000-112241	20000607
	EP 1065717	A3	20030820		
	JP 2001015929	A2	20010119	JP 1999-183375	19990629
	JP 3213291	B2	20011002		
	US 6399891	**B1**	**20020604**	**US 2000-587386**	**20000605**
	TW 530395	B	20030501	TW 2000-89110953	20000605
	CN 1279157	A	20010110	CN 2000-118480	20000628
PRAI	JP 1999-183375	A	19990629		

AB A multilayer board comprising **alternating polyimide films** and copper films is fabricated, which is free from breakage at connecting parts due to thermal fatigue. The polyimide films have a thermal expansion coefficient of 2-5 ppm/°C so that the multilayer board has a total thermal expansion coefficient of less than **10** ppm/°C. Because of the thermal expansion coefficient close to that of the semiconductor element to be mounted, no breakage occurs at connecting parts to the semiconductor element. The multilayer board of the present invention may be used as both **interposer** and motherboard.

IT Acrylic polymers, uses
Epoxy resins, uses
Polyimides, uses
(resin layers; multilayer circuit boards free from breakage due to thermal fatigue)
IT 7440-22-4, Silver, uses 7440-50-8, Copper, uses 7440-57-5, Gold, uses
(conductive films; multilayer circuit boards free from breakage due to thermal fatigue)
IT **89-32-7**, Pyromellitic anhydride
(polyimide film formation from reaction between an acid and an amine)
RN 89-32-7 HCAPLUS
CN 1H,3H-Benzo[1,2-c:4,5-c']difuran-1,3,5,7-tetrone (9CI) (CA INDEX NAME)



L70 **ANSWER** 4 OF 6 **HCAPLUS COPYRIGHT ACS on STN**
AN 2000:814774 HCAPLUS Full-text
DN 133:358177
ED Entered STN: 21 Nov 2000
TI Method for manufacturing a printed circuit board with integrated heat sink for semiconductor package
IN Juskey, Frank J.; McMillan, John R.; Huemoeller, Ronald P.
PA Amkor Technology, Inc., USA

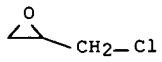
	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000069239	A1	20001116	WO 2000-US13041	20000511
	US 6337228	**B1**	**20020108**	**US 1999-310660**	**19990512**
	US 2002043402	**A1**	**20020418**	**US 2001-6642**	**20011205**
	US 6507102	**B2**	**20030114**		
PRAI	US 1999-310660	A	19990512		

AB A low-cost printed circuit board (10) for a semiconductor package having the footprint of a **ball grid array** package has an integral heat sink (20), or slug, for the mounting of one or more semiconductor chips, capable of efficiently conducting away at least five watts from the package in typical applications. It is made by forming an opening (16) through a sheet, or substrate (14), of B-stage epoxy/fiberglass composite, or pre-preg, then inserting a slug (20) of a thermally conductive material having the same size and shape as the opening into the opening. The slug-containing composite is sandwiched **between** two **thin** layers (30) of a conductive metal, preferably Cu, and the resulting sandwich (10) is simultaneously pressed and heated between the platen (12) of a heated press. The heat and pressure forces the **resin** to the surface of the composite (10) and into the space between the slug (20) and the walls of the composite, where it solidifies, bonding the edges of the slug (20) to the substrate (14) within the opening and adhering the conductive layers (30) to the upper and lower surfaces of the substrate (14). The resulting laminate (10) can thereafter be processed as a convention printed circuit board to incorporate conventional circuit board features, e.g., circuit traces, wire bonding pads, solder **ball** mounting lands, and via holes.

IT Polyimides, processes
(**bismaleimide**-based, **triazine** group-containing; manufacturing printed circuit board with integrated heat sink for semiconductor package)
IT Epoxy **resins**, processes
Polyimides, processes
(manufacturing printed circuit board with integrated heat sink for semiconductor package)
IT **25068-38-6**, Epichlorohydrin-bisphenol A copolymer
(manufacturing printed circuit board with integrated heat sink for semiconductor package)
RN 25068-38-6 HCAPLUS
CN Phenol, 4,4'-(1-methylethylidene)bis-, polymer with (chloromethyl)oxirane

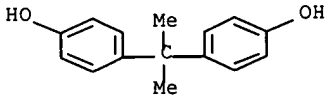
CM 1

CRN 106-89-8
CMF C3 H5 Cl O



CM 2

CRN 80-05-7
CMF C15 H16 O2



L70 **ANSWER** 5 OF 6 **HCAPLUS COPYRIGHT ACS on STN**
AN 2000:748892 HCAPLUS Full-text
DN 133:322745
ED Entered STN: 24 Oct 2000
TI Liquid **epoxy resin** compositions for under-filling materials of **flip chip**-type semiconductor devices
IN Shiohara, Toshio; Sumida, Kazumasa
PA Shin-Etsu Chemical Industry Co., Ltd., Japan

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2000297202	A2	20001024	JP 2000-23749	20000201
US 6310120	**B1**	**20011030**	**US 2000-499038**	**20000207**

PRAI JP 1999-33731 A 19990212

AB The compns. contain (a) 100 parts liquid **epoxy resins**, (b) 0-100 parts hardeners, (c) 0.01-10 parts (to a + b 100 parts) SiO2 microspheres, (d) soft x-ray-shielding globular inorg. fillers of the amount being ED to shield soft x-ray, and (e) 0.01-10 parts (to a + b 100 parts) curing accelerators. Thus, a composition with gel time at 150° 65 s comprised bisphenol A **epoxy resin** (RE 310) 50, methyltetrahydrophthalic anhydride (Rikacid MH 700) 40, SO 32H (SiO2) 150, 50:50 SiO2-ZrO composite 50, (γ-glycidoxypropyl)trimethoxysilane (KBM 403) 0.2, and an **imidazole**-containing microcapsule (HX 3741) 3 parts. The composition exhibited excellent permeation to a **thin** gap **between** polyimide films. Void existence or nonexistence in a semiconductor packaged with the composition could be easily detected with soft x-ray irradiation

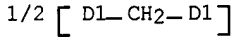
IT **Epoxy resins**, uses
(liquid **epoxy resin** compns. for under-filling materials of **flip chip**-type semiconductor devices)

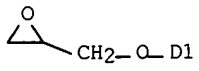
IT **96141-20-7**, RE 304
(liquid **epoxy resin** compns. for under-filling materials of **flip chip**-type semiconductor devices)

RN 96141-20-7 HCAPLUS
CN Oxirane, 2,2'-[methylenebis(phenyleneoxymethylene)]bis-, homopolymer (9CI)

CM 1

CRN 39817-09-9
CMF C19 H20 O4
CCI IDS





L6 **ANSWER** 6 OF 15 **WPIX COPYRIGHT THOMSON DERWENT on STN**
AN 2001-564146 [63] WPIX Full-text
CR 2000-181367 [16]
DNC C2001-167369
TI Semiconductor chip assembly includes compliant **interposer** layer having flexible conductive **polymer** electrically connecting contacts on die to bond pads on dielectric substrate wiring layer.
IN GILLEO, K B; GRUBE, G W; MATHIEU, G
PA (TESS-N) TESSERA INC
PI US 6252301 B1 20010626 (200163)* 8 H01L023-52 <--
PRAI US 1996-21412P 19960709; US 1996-709470 19960905;
US 1999-450252 19991129
IC ICM **H01L023-52**
AB US 6252301 B UPAB: 20011031
NOVELTY - A semiconductor chip assembly includes a compliant interposer layer mechanically coupling a face surface of a die and a face surface of a **dielectric** substrate. The compliant **interposer** at least partially comprises a flexible conductive polymer electrically connecting contacts on the die to bond pads on the first surface of the dielectric substrate.

DETAILED DESCRIPTION - A semiconductor chip assembly comprises a semiconductor die (100) having a face surface (130) bearing contacts (150). A dielectric substrate wiring layer (120) juxtaposed with the die has a first surface having conductive bond pads in rough alignment with the contacts on the die and a second surface having conductive terminals (160). The bond pads are electrically connected to the terminals. A compliant interposer layer (110) mechanically couples the face surface of the die and the first surface of the **dielectric** substrate. The compliant **interposer** is at least partially composed of a flexible conductive polymer (190) electrically connecting the contacts to respective bond pads. The compliant interposer is compliant enough to mechanically decouple the shear forces due mainly to the coefficient of thermal expansion mismatch acting on a resulting chip package during operation.

USE - As semiconductor chip assembly.

ADVANTAGE - Compliancy in the interposer layer and in the conductive polymer permits movement of the terminals on the die, and thus relieves the shear forces caused by differential thermal expansion. The invention provides a compact packaged structure similar to that achieved through flip-chip bonding, but with increased resistance to thermal cycling damage. It allows standardization of the package such that companies can make competing chips that are packaged such that the resultant packaged structures are roughly the same as far as the end user is concerned.

DESCRIPTION OF DRAWING(S) - The figure shows a side view of a compliant semiconductor chip package.

Semiconductor die 100
Compliant interposer layer 110
Dielectric substrate wiring layer 120 Face surface 130
Contacts 150
Terminals 160
Conductive polymer 190

TECH US 6252301 B1 UPTX: 20011031
TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The compliant interposer layer comprises entirely out of a compliant anisotropic conductive layer which conducts in an approximate axial direction from the contacts to their respective bond pads. The compliant conductive layer is biased to conduct between desired adjacent contacts. The compliant further comprises apertures which are aligned with the contacts and bond pads. The conductive polymer is disposed within the apertures and is electrically connected between contacts and bond pads. A conductive contact interface is coupled to the contact on the die, and functions on ensuring the conductivity of the contact.

TECHNOLOGY FOCUS - **POLYMERS** - Preferred Materials: The compliant **interposer** layer comprises silicones, flexible **epoxies**, gels, fluoropolymers, or foams. The conductive polymer is silver filled epoxy, silver filled silicone resin, or silver filled polysiloxane-polyimide.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The contact interface is a gold layer, gold bump, gold post, conductive adhesive, or ball bonded gold wire bond.

L6 **ANSWER** 7 OF 15 **WPIX COPYRIGHT THOMSON DERWENT on STN**
AN 2001-323735 [34] WPIX Full-text
DNN N2001-233302
TI Ball grid array type semiconductor device has alloy layer of solder bump and bump electrode material on boundary surface of solder bump and bump electrode.
DC U11
IN IIJIMA, M; MORIOKA, M; NUKIWA, M; UENO, S
PA (FUIT) FUJITSU LTD
CYC 3
PI JP 2001085470 A 20010330 (200134)* 9 H01L021-60
US 6396155 B1 20020528 (200243) **H01L023-48** **<--**
TW 464992 A 20011121 (200248) H01L021-60
ADT JP 2001085470 A JP 1999-262007 19990916; US 6396155 B1 US 2000-605086 20000627; TW 464992 A TW 2000-113325 20000705
PRAI JP 1999-262007 19990916
IC ICM H01L021-60; **H01L023-48**
AB JP2001085470 A UPAB: 20010620
NOVELTY - A bump electrode (27) is inserted in a solder bump (12) formed on semiconductor device (1). An alloy layer of solder bump material and bump electrode material are formed on the boundary surface of solder bump and bump electrode. **Insulated resin** (17) is **interposed** between semiconductor device and substrate (20) in which bump electrode is connected.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for semiconductor device manufacture.

USE - Ball grid array type semiconductor device.

ADVANTAGE - Connection reliability of bump and bump electrode is improved, thereby manufacturing efficiency is improved. Mechanical bondability and electric connectability are improved by alloy layer. Since arrangement of solder ball on substrate and formation of alloy layer are carried out simultaneously, processing time is shortened and manufacturing cost is reduced. Since bump electrode breaks insulating film currently formed on bump surface, degradation of electric connectability of bump and bump electrode is prevented.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of semiconductor device. (The drawing includes non-English language text).

Semiconductor device 1
Solder bump 12
Alloy layer 18
Insulated resin 17
Substrate 20
Bump electrode 27

L32 ANSWER 2 OF 2 **HCAPLUS COPYRIGHT ACS on STN**
AN 2000:900975 HCAPLUS Full-text
DN 134:64919
ED Entered STN: 22 Dec 2000
TI High density metal layer substrate for circuit boards and methods for manufacturing same
IN Smith, Gordon; Gotro, Jeffrey T.; Hein, Marc; Androff, Nancy M. W.
PA Alliedsignal Inc., USA

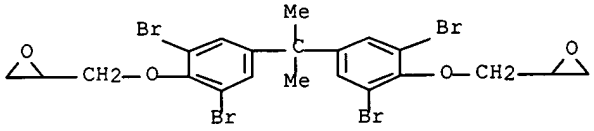
	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000078107	A1	20001221	WO 2000-US16220	20000614
	EP 1190606	A1	20020327	EP 2000-939835	20000614
	JP 2003501301	T2	20030114	JP 2001-502628	20000614
PRAI	**US 1999-332619**	**A**	**19990614**		
	WO 2000-US16220	W	20000614		

AB This invention concerns **ultra-thin** metal layer containing substrates useful for manufacturing high d. circuits as well as novel methods for using the substrates to manufacture laminates, circuits, interposers, and other electronic laminates.

IT **Polyimides**, processes **(Upilex**; high d. metal layer substrate for circuit boards and methods for manufacturing same)
IT 7440-57-5, **Gold**, processes
(high d. metal layer substrate for circuit boards and methods for manufacturing same)
IT **33294-14-3, Quatrex 6410**
(high d. metal **layer** substrate for circuit boards and methods for manufacturing using)
RN 33294-14-3 HCAPLUS
CN Oxirane, 2,2'-[(1-methylethylidene)bis[(2,6-dibromo-4,1-phenylene)oxymethylene]]bis-, homopolymer (9CI) (CA INDEX NAME)

CM 1

CRN 3072-84-2
CMF C21 H20 Br4 O4



65/9/2
DIALOG(R) File 2: INSPEC

6730475 INSPEC Abstract Number: B2000-11-0170J-179
Title: Guidelines to select underfills for **flip** chip on board assemblies and compliant **interposers** for chip scale package assemblies
Author(s): Okura, J.H.; Shetty, S.; Ramakrishnan, B.; Dasgupta, A.; Caers, J.F.J.M.; Reinikainen, T.
Author Affiliation: CALCE Electron. Products & Syst. Consortium, Maryland Univ., College Park, MD, USA
Journal: Microelectronics Reliability vol.40, no.7 p.1173-80
Publisher: Elsevier,
Publication Date: July 2000 Country of Publication: UK
CODEN: MCRLAS ISSN: 0026-2714
SICI: 0026-2714(200007)40:7L.1173:GSUF;1-5
Material Identity Number: G489-2000-006
U.S. Copyright Clearance Center Code: 0026-2714/2000/$20.00
Document Number: S0026-2714(00)00044-5
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Theoretical (T)
Abstract: The effect of thermomechanical properties of underfill and compliant interposer materials, such as CTE and stiffness (Young's modulus) on the reliability of **flip chip** on board (FCOB) and CSPs under thermal cycling stresses is investigated in this study. Quasi-3D viscoplastic stress analysis using finite element modeling (FEM) is combined with an energy partitioning model for creep-fatigue damage accumulation to predict fatigue durability for a given thermal cycle. Parametric FEM simulations are performed for five different CTEs and five different stiffnesses of the underfill and compliant interposer materials. The creep work dissipation due to thermal cycling is estimated with a quasi 3D model, while a 3D model is used to estimate the hydrostatic stresses. To minimize the computational effort, the 3D analysis is conducted only for the extreme values of the two parameters (CTE and stiffness) and the results are interpolated for intermediate values. The results show that the stiffness and CTE of the underfill material play an important role in influencing FCOB assembly fatigue life. Fatigue durability increases as underfill stiffness and CTE increase. In the case of compliant interposers, the reverse is true and durability increases as interposer stiffness decreases. Furthermore, interposer CTE affects fatigue durability more significantly than underfill CTE, with durability increasing as CTE decreases. The eventual goal is to define the optimum design parameters of the FCOB underfill and CSP interposer, in order to maximize the fatigue endurance of the solder joints under cyclic thermal loading environments.

65/9/3
DIALOG(R) File 2: INSPEC

6715237 INSPEC Abstract Number: B2000-11-0170J-046
Title: Silicon **interposer** technology for high-density package
Author(s): Matsuo, M.; Hayasaka, N.; Okumura, K.; Hosomi, E.; Takubo, C.
Author Affiliation: ULSI Process Eng. Lab., Toshiba Corp., Yokohama, Japan
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference (Cat. No.00CH37070) p.1455-9
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xxxv+1756 pp.
ISBN: 0 7803 5908 9 Material Identity Number: XX-2000-01366
U.S. Copyright Clearance Center Code: 0 7803 5908 9/2000/$10.00
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, and Manuf. Technol. Soc. of IEEE; Electronic Ind. Alliance
Conference Date: 21-24 May 2000 Conference Location: Las Vegas, NV,
Language: English Document Type: Conference Paper (PA)
Treatment: New Developments (N); Experimental (X)
Abstract: The achievement of rapid advances in integration density and performance of LSI devices is predicated on increasing the total number of Input/Output (I/O) and Power/Ground (P/G) terminals, which, in turn, leads to shrinking design rule of wiring and **bump** pitch on the organic substrate of a **flip**-chip package. However, decreasing the **bump** pitch and wiring rule raises the process cost of fabricating organic substrate. Moreover, it is difficult to obtain highly reliable connections between chip and organic substrate with smaller **bumps** due to the mismatching of the coefficient of the thermal expansion (CTE). To overcome these problems, a new interposer using silicon (Si) substrate with through plug is developed. (3 Refs)

L69 **ANSWER** 6 OF 7 **HCAPLUS COPYRIGHT ACS on STN**
AN 2000:748892 HCAPLUS Full-text
DN 133:322745
ED Entered STN: 24 Oct 2000
TI Liquid **epoxy resin** compositions for under-filling materials of flip chip-type semiconductor devices
IN Shiohara, Toshio; Sumida, Kazumasa
PA Shin-Etsu Chemical Industry Co., Ltd., Japan
IC ICM C08L063-00
ICS C08G059-20; C08K003-22; C08K003-36; **H01L021-60**; **H01L023-29**; **H01L023-31**

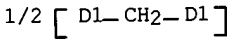
PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000297202	A2	20001024	JP 2000-23749	20000201
US 6310120	**B1**	**20011030**	**US 2000-499038**	**20000207**
PRAI JP 1999-33731	A	19990212		

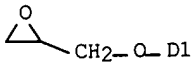
AB The compns. contain (a) 100 parts liquid **epoxy resins**, (b) 0-100 parts hardeners, (c) 0.01-10 parts (to a + b 100 parts) SiO2 microspheres, (d) soft x-ray-shielding globular inorg. fillers of the amount being ED to shield soft x-ray, and (e) 0.01-10 parts (to a + b 100 parts) curing accelerators. Thus, a composition with gel time at 150° 65 s comprised bisphenol A **epoxy resin** (RE 310) 50, methyltetrahydrophthalic anhydride (Rikacid MH 700) 40, SO 32H (SiO2) 150, 50:50 SiO2-ZrO composite 50, (γ-glycidoxypropyl)trimethoxysilane (KBM 403) 0.2, and an **imidazole**-containing microcapsule (HX 3741) 3 parts. The composition exhibited excellent permeation to a **thin** gap **between** polyimide films. Void existence or nonexistence in a semiconductor packaged with the composition could be easily detected with soft x-ray irradiation

IT **Epoxy resins**, uses
(liquid **epoxy resin** compns. for under-filling materials of flip chip-type semiconductor devices)
IT **96141-20-7**, RE 304
(liquid **epoxy resin** compns. for under-filling materials of flip chip-type semiconductor devices)
RN 96141-20-7 HCAPLUS
CN Oxirane, 2,2'-[methylenebis(phenyleneoxymethylene)]bis-, homopolymer (9CI) (CA INDEX NAME)

CM 1

CRN 39817-09-9
CMF C19 H20 O4
CCI IDS





L6 **ANSWER** 8 OF 15 **WPIX COPYRIGHT THOMSON DERWENT on STN**
AN 2001-201380 [20] WPIX Full-text
CR 2002-349966 [38]
DNN N2001-143486
TI Stacked packaging structure for integrated circuits in computer, consists of space between IC chip and rigid **interposer**, filled with **polymer** having electrically insulating thermally conductive powder.
DC T01 U11 U14
IN CHAN, M Y; LOW, S W; YEW, C K
PA (TEXI) TEXAS INSTR INC
CYC 1
PI US 6137164 A 20001024 (200120)* 10 H01L023-02 <--
ADT US 6137164 A Provisional US 1998-78056P 19980316, US 1999-401568 19990922
PRAI US 1998-78056P 19980316; US 1999-401568 19990922
IC ICM **H01L023-02**
AB US 6137164 A UPAB: 20030716
NOVELTY - The packaging structure includes IC chips (803,804) mounted face to face on surfaces (882,881) of a rigid interposer (880). The perimeter of the structure is made slightly greater than the larger chip and the thickness is set to be in the range of 1.25-1.5mm. The space between the chips and interposer is filled with an under fill polymer formulated with electrically insulating thermally conductive powder.

DETAILED DESCRIPTION - The surfaces of the interposer have printed wiring circuitry of more than two levels. The electrical terminals of the chips are electrically and mechanically connected to contacts pads on the interposer surfaces, by anisotropic conductive adhesive with low alpha emissivity. The IC terminals are electrically connected to conductive vias between the interposer surfaces, by printed metal traces on the interposer. The vias terminate in external connectors comprising solder balls (841), at lower surface of packaging structure.

USE - For integrated circuits such as single inline memory module (SIMM), 64 MB DRAMs, digital signal processor, microprocessor used in computers and other portable systems.

ADVANTAGE - Provides a very thin IC packaging structure with improved packing density and performance of integrated circuit devices. The provision of rigid interposer allows two chips to be directly attached to the interposer and to external contacts. Since interposer comprises low cost circuit board material that is readily available, rapid and cost effective production of IC package is enabled. Since the space between the chips and **interposer** is filled with underfill **polymer** formulated with electrically insulating thermally conductive power, stresses on contact joints are mitigated and thereby thermal dissipation from chip surface is enhanced which in turn protects against ingress of moisture and other contaminants.

DESCRIPTION OF DRAWING(S) - The figure shows the cross sectional view of packaging structure of IC chips. IC chips 803,804
Solder ball 841
Interposer 880
Surfaces of interposer 881,882 Dwg.8/8

L6 **ANSWER** 9 OF 15 **WPIX COPYRIGHT THOMSON DERWENT on STN**
AN 2001-097091 [11] WPIX Full-text
DNN N2001-073917
TI Circuit board for resin sealed semiconductor device, has electrically insulative resin layer or formed between external frame, die pad and terminals.
DC U11
PA (NIPQ) DAINIPPON PRINTING CO LTD
CYC 1
PI JP 2000332145 A 20001130 (200111)* 11 H01L023-12 <--
ADT JP 2000332145 A JP 1999-136703 19990518
PRAI JP 1999-136703 19990518
IC ICM **H01L023-12**
ICS H01L023-50
AB JP2000332145 A UPAB: 20010224
NOVELTY - The circuit board has electrically **insulative resin** layer (5) **interposed** between at external frame (2), a die pad (3) and each of the terminals (4) formed inside the frame and arranged to the planar surface independently. The internal and external terminal surface of terminals are exposed so that a recess is formed between the resin layer.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included following:

(a) resin sealed semiconductor device;

(b) circuit board manufacturing method

USE - For resin sealed semiconductor devices e.g. application specific integrated circuits used in electrical equipments.

ADVANTAGE - Provides size reduction and increased package density to circuit board. The circuit board is reinforced by the resin. Deformation of the circuit boards is prevented. Enables manufacture of ball grid array semiconductor device. Mounting operativity is improved. Attains correspondence to multi pin formation.

DESCRIPTION OF DRAWING(S) - The figure shows the cross sectional view of the circuit board.

External frame 2
Die pad 3
Terminals 4
Resin layer 5

L6 **ANSWER** 10 OF 15 **WPIX COPYRIGHT THOMSON DERWENT on STN**
AN 2001-055586 [07] WPIX Full-text
DNN N2001-043091
TI Chip size package has external terminal lands with solder balls which are exposed through opening in **insulated resin** sheet of **interposer.**
DC U11
PA (MIHI) MITSUI HIGH TEC KK
CYC 1
PI JP 2000315745 A 20001114 (200107)* 5 H01L023-12 <--
ADT JP 2000315745 A JP 1999-124152 19990430
PRAI JP 1999-124152 19990430
IC ICM **H01L023-12**
AB JP2000315745 A UPAB: 20010202
NOVELTY - The electrode pads (13) provided on IC chip (11) surface are connected to terminal leads (14). A lead frame (16) of the chip is provided with conductor lead (15) and external terminal lands (19). The external terminal lands provided with solder ball (21) are exposed through an opening in **insulated resin** sheet (20) of **interposer** (12). A sealing **resin** (23) seals the chip.

DETAILED DESCRIPTION - Electrode pads are deposited in center or around edges of chip surface. The lead frame of chip is fabricated by stamping operation. Chip is sealed partially or completely with sealing resin.

USE - For providing **interposer** with **insulated resin** sheet in CSP type semiconductor device.

ADVANTAGE - Since it is unnecessary to use polyimide resin tape, and opening which exposes external connecting terminal lands can be easily formed by exposure and development, portable semiconductor device is cheaply manufactured.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of semiconductor device.
Interposer 12
Electrode pads 13
Terminal leads 14
Conductor lead 15
Lead frame 16
Terminal lands 19
Resin sheet 20
Solder ball 21
Sealing resin 23

36/9/6
DIALOG(R) File 2: INSPEC

6777156 INSPEC Abstract Number: B2001-01-0170J-074
Title: Flex, rigid, and ceramic CSP-lifetime behavior
Author(s): Albrecht, H.-J.; Jendrny, J.; Muller, W.H.; Schwarz, B.; Teichmann, H.; Tilgner, R.
Author Affiliation: Siemens AG, Berlin, Germany
Conference Title: Pan Pacific Microelectronics Symposium. Proceedings of the Technical Program p.331-44
Publisher: Surface Mount Technol. Assoc, Edina, MN, USA
Publication Date: 2000 Country of Publication: USA 423 pp.
Material Identity Number: XX-2000-01481
Conference **Title:** Proceedings of Fifth Annual Pan Pacific Microelectronics Symposium
Conference Sponsor: GPD
Conference Date: 25-27 Jan. 2000 Conference Location: Maui, HI, USA
Language: English Document Type: Conference Paper (PA)
Abstract: This paper presents a detailed numerical, nonlinear finite element (FE) analysis of three different CSPs which use PI flex, an alumina ceramic, or a **BT resin as interposer** material. Lifetime predictions (number of cycles to failure) are carried out on the basis of equivalent creep strains accumulated during thermal cycle tests (TCTs). Moreover, the development of temperature profiles under power cycle tests (PCTs) is simulated and used to predict the resulting irreversible strains within the solder bumps. The predictions from FE simulations are finally compared to reliability experiments (TherMoire/sup R/ displacement measurements, Weibull plots of board level reliability, and distributions of crack lengths). (20 Refs)

65/9/1
DIALOG(R) File 2: INSPEC

6858061 INSPEC Abstract Number: B2001-04-0170J-026
Title: **Polyimide** flexible **interposer** for CSP (chip size/scale package)
Author(s): Iwasaki, Y.; Hasegawa, K.; Tobe, T.; Takeuchi, K.; Tsubomatsu, Y.; Yusa, M.; Inoue, F.
Author Affiliation: Hitachi Chem. Co. Ltd., Ibaraki, Japan
Publication Date: Proceedings. Electronic Circuits World Convention 8 p.H4da-b, H4de
Publisher: Electronics Circuits World Convention 8, Birmingham, UK
Publication Date: 1999 Country of Publication: UK CD-ROM pp.
Material Identity Number: XX-1999-03090
Publication Date: Proceedings of Electronic Circuits World Convention
Conference Sponsor: Japan Printed Circuit Assoc.; Eur. Inst. of Printed Circuits; Assoc. Connecting Electron. Ind
Conference Date: 7-10 Sept. 1999 Conference Location: Tokyo, Japan
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: Portable electronic appliances are rapidly being upgraded and miniaturized. To keep abreast of this, miniature LSI packages have been developed and the CSP (chip size/scale package) is now in the final stages of development. Using various insulating material technologies and fine pitch patterning technology, we have developed a film type interposer for the CSP. This interposer is a simple structure with a polyimide film which has patterns on one side and has openings on the other side for solder **ball** attachment. The base material consists of a commercial polyimide core film and developed adhesive layers on both sides in order to reduce warpage of the interposer. Our electroless gold-plating process is adopted for plating of the wire-bonding terminals. This process results in uniform fine wiring and excellent wire bondability. Furthermore, by fabricating vent holes in the interposer and placing the newly developed die-bonding film on the interposer, we can maintain excellent reflow resistance.

L8 ANSWER 2 OF 2 **HCAPLUS COPYRIGHT ACS on STN**
AN 1997:270602 HCAPLUS Full-text
DN 126:252451
ED Entered STN: 28 Apr 1997
TI **Cyanate ester resin films** that promote metal-plating adhesion to cyanate ester resin-graphite composites
IN Punsly, Brian M.; Wong, Thomas G.
PA Hughes Electronics, USA

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 759329	A2	19970226	EP 1996-111879	19960724
	EP 759329	A3	20020717		
	US 6080836	**A**	**20000627**	**US 1997-822203**	**19970320**
PRAI	US 1995-507178	A	19950726		

AB A layer consisting essentially of cyanate ester resin is applied to the surface of the composite. Thereafter, the surface of the resin layer is etched, preferably by treatment with an etching solution containing either a quaternary ammonium hydroxide or a primary amine. Upon completion of the etching process, the resin layer is plated with a conductive metal. The method of the invention operates to improve adhesion between the resin composite and a subsequently-plated metal by providing the composite with a homogeneous distribution of mech. anchoring sites for a subsequently-plated metal, such that uniformity of adhesion is achieved. A cyanate ester resin composite prepared for plating in accordance with the invention may, upon plating, replace certain metallic components in such applications as aircraft, spacecraft, and automobiles given its highly conductive metallic coating.

IT **188653-06-7**, RS 12 (cyanate ester)
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(cyanate ester resin; cyanate ester resin **films** that promote metal-plating adhesion to cyanate ester resin-graphite composites)

L6 **ANSWER** 11 OF 15 **WPIX COPYRIGHT THOMSON DERWENT on STN**
AN 2000-115265 [10] WPIX Full-text
CR 2001-272762 [25]; 2002-163618 [06]
DNN N2000-087150
TI Semiconductor chip mounting interposer in microelectronic components used in electronic devices.
DC U11
IN BELLAAR, P H; DISTEFANO, T H; FJELSTAD, J; PICKETT, C M; SMITH, J W
PA (TESS-N) TESSERA INC
CYC 1
PI US 6002168 A 19991214 (200010)* 10 H01L023-48 <--
ADT US 6002168 A US 1997-978082 19971125
PRAI US 1997-978082 19971125
IC ICM **H01L023-48**
ICS H01L023-06; H01L023-52
AB US 6002168 A UPAB: 20020403
NOVELTY - The terminals are disposed on the top surface of the flexible interposer. The electrical contacts are electrically interconnected to the terminals with flexible electrical connections. Several joining units disposed on the terminals, are electrically connected to the terminals. Each joining unit includes a spherical solid core.

DETAILED DESCRIPTION - The rigid interposer has first and second surfaces and electrical contacts on the second surface. The flexible interposer has a top surface, bottom surface and terminals disposed on top surface. The top surface faces the second surface while the bottom surface faces away from the surface at rigid interposer. The rigid **interposer** comprises a rigid **dielectric** material selected from the group consisting of alumina, beryllia, silicon carbide, aluminum nitride, forsterite, mullite, glass ceramics, polyester-fiber glass, **polyimide**-fiber glass, **epoxy**-fiber glass. The flexible **interposer** comprises a **flexible sheet of polymeric material**.

USE - For mounting semiconductor chip of microelectronic component such as resistor, inductor, capacitor, etc. used in electronic devices.

ADVANTAGE - The flexible interposer facilitates movement of the contact ends of the leads relative to the terminals and thus contributes to the ability of the chip carrier to withstand thermal cycling.

DESCRIPTION OF DRAWING(S) - The figure shows diagrammatic sectional view of semiconductor chip assembly. Dwg.2,3/3

33/9/13
DIALOG(R) File 2: INSPEC

6736775 INSPEC Abstract Number: B2000-12-0170J-007
Title: Flip chip wafer level packaging of a flexible chip scale package (CSP)
Author(s): Hotchkiss, G.; Amador, G.; Edwards, D.; Hundt, P.; Stark, L.; Stierman, R.; Heinen, G.
Author Affiliation: Texas Instrum. Inc., Dallas, TX, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3906 p.555-62
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1999 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1999)3906L.555:FCWL;1-J
Material Identity Number: C574-2000-070
Publication Date: 1999 International Symposium on Microelectronics
Conference Sponsor: IMAPS
Conference Date: 26-28 Oct. 1999 Conference Location: Chicago, IL, USA
Language: English Document Type: Conference Paper (PA); Journal Paper
Treatment: Applications (A); Practical (P); Theoretical (T)
Abstract: The advent of chip scale packages (CSP) within the semiconductor community has led to the development of wafer scale assembly (WSA) or wafer level packaging (WLP) manufacturing in order to raise assembly efficiencies and lower operating costs. Texas Instruments (TI) has developed a unique WLP process for forming **flip chip, ball grid array** packages. The die inputs and outputs of the TI CSP are connected through solder **bumps** to a **polyimide film interposer**. Solder balls on the other side of the **interposer** complete the electrical connection to a customer's printed circuit board. A wafer-sized array of **interposers** designed to match the pattern of dies on a wafer is aligned and reflowed to a **bumped** wafer. The TI WLP process is completed by singulating the CSP's from the wafer using standard wafer saw equipment. Attachment of the **interposer** to the die as well as applying the die and board level solder **bumps** are carried out in wave form using a new bumping technology called Tacky Dots/sup TM/. Tacky Dots uses an array of sticky dots formed in a photosensitive coating laminated to a polymide film for transferring and attaching solder spheres to semiconductor substrates. A populated film containing one solder sphere per tacky dot is positioned over the wafer or **interposer** and lowered until the spheres contact the **pads**. A reflow process transfers the spheres from the **film** to the wafer or **interposer** and the **film** is removed once the spheres have frozen. This paper illustrates the process steps and custom equipment developed for forming the TI CSP. The strategic use of finite element modeling for optimizing the design of the package is outlined. The paper concludes by summarizing the current package level reliability results. (8 Refs)

L50 ANSWER 3 OF 3 **HCAPLUS COPYRIGHT ACS on STN**
AN 1999:359391 HCAPLUS Full-text
DN 131:123619
ED Entered STN: 11 Jun 1999
TI New high-density multilayer technology on **PCB**
AU Shimoto, Tadanori; Matsui, Koji; Kikuchi, Katsumi; Shimada, Yuzo; Utsumi, Kazuaki
CS Functional Materials Research Laboratories, NEC Corporation, Kanagawa, 216, Japan
SO IEEE Transactions on Advanced Packaging (1999), 22(2), 116-122
CODEN: ITAPFZ; ISSN: 1521-3323
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB Demand has recently increased for very high-d. packaging substrates for high-pin-count area array chips. The authors' new high-d. multilayer technol. on **printed circuit board** (**PCB**), named deposited substrate on laminate (DSOL) satisfies this demand. An important feature of the DSOL is dielec. fabrication, which uses a new photosensitive material; an aromatic fluorene unit bonded epoxy acrylate resin. The fluorene based resin has interesting properties such as good elec. properties, low curing temperature (160°) for a heat-resistant resin (glass transition temperature, Tg = 230°), low coefficient of the thermal expansion (40 ppm), and excellent via hole resolution Very fine and high-aspect-ratio (>1.0) via holes were formed through exactly the same process steps as those used for a conventional photosensitive epoxy resin; baking, exposure, and development with an aqueous alkaline solution Another important feature is the technol., that patterns fine-pitch Cu conductors using a semi-additive process with a sputtering method. The DSOL made 40 μm very fine pitch Cu conductors on large laminates (330 mm + 400 mm) possible, because this process was composed of flash wet etching of only 0.3 μm thick sputtered **thin-films**. The authors have successfully developed a high-d. packaging substrate for high-pin-count (4000 pins) area array application specific integrated circuit (ASIC) chips.

35/9/8
DIALOG(R) File 2: INSPEC

6044845 INSPEC Abstract Number: B9811-4260D-027
Title: **Ultrathin** self-assembled layers at the ITO interface to control charge injection and electroluminescence efficiency in **polymer** light-emitting diodes
Author(s): Ho, P.K.H.; Granstroem, M.; Friend, R.H.; Greenham, N.C.
Author Affiliation: Cavendish Lab., Cambridge Univ., UK
Journal: Advanced Materials vol.10, no.10 p.769-74
Publisher: VCH Verlagsgesellschaft,
Publication Date: **9 July 1998** Country of Publication: Germany
CODEN: ADVMEW ISSN: 0935-9648
SICI: 0935-9648(19980709)10:10L.769:USAL;1-S
Material Identity Number: M606-98013
Language: English Document Type: Journal Paper (JP)
Treatment: Experimental (X)
Abstract: Modification of polymer LED operating characteristics has been achieved by **interposing** a conducting, semi-conducting, or **insulating polymer layer** at the interface between the indium tin oxide (ITO) electrode and the emissive polymer. The figure shows schematically a conducting polymer interlayer (sulfonated polyaniline and hexadimethrine polymer) fabricated by the polyelectrolyte self-assembly technique. (27 Refs)

35/9/9
DIALOG(R) File 2: INSPEC

5928914 INSPEC Abstract Number: B9807-0170J-034
Title: High pin count and high-frequency operation LSI package for ASIC
Author(s): Yajima, K.; Nakao, H.; Kajihara, M.; Dobashi, M.; Baba, M.; Furuya, K.
Author Affiliation: Syst. ASIC Div., NEC Corp., Japan
Journal: NEC Technical Journal vol.51, no.3 p.103-5
Publisher: NEC,
Publication Date: March 1998 Country of Publication: Japan
CODEN: NECGEZ ISSN: 0285-4139
SICI: 0285-4139(199803)51:3L.103:HCHF;1-W
Material Identity Number: H719-98006
Language: Japanese Document Type: Journal Paper (JP)
Treatment: Applications (A); Practical (P)
Abstract: NEC has developed the Flip Chip **Ball** Grid **Array** (FCBGA) package for high pin count and high-frequency operation ASICs of 0.25 micron and more advanced generation. This package has **an organic substrate as an interposer,** high melting point solder **bump** with eutectic solder as the connection between die and substrate, and underfill resin and heat spreader which are directly placed on the backside of the die for power dissipation. This package also achieves long-term reliability. (0 Refs)

L42 ANSWER 2 OF 2 **HCAPLUS COPYRIGHT ACS on STN**
AN 1998:678595 HCAPLUS Full-text
DN 130:31563
ED Entered STN: 28 Oct 1998
TI Semiconductor chip packaged in a modified encapsulant
AU Anon.
CS UK
SO Research Disclosure (1998), 414(Oct.), P1310 (No. 41409)
CODEN: RSDSBB; ISSN: 0374-4353
PB Kenneth Mason Publications Ltd.
DT Journal; Patent
LA English
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 38

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI RD 414009		**19981010**		

PRAI RD 1998-414009 19981010

AB An electronic package is described which improves the reliability between an Si chip and a **PCB**. This package contains a flexible **interposer** and a complaint layer (silicone or epoxy resin) over the chip. The silicone encapsulant may contain fillers.

IT Epoxy **resins**, uses

67/9/1
DIALOG(R) File 2: INSPEC

6232718 INSPEC Abstract Number: B1999-06-0170J-019
Title: Flexible **polyimide interposer** for CSP preparation
Author(s): Beyer, V.; Kuchenmeister, F.; Bottcher, M.; Meusel, E.
Author Affiliation: Semicond. Technol. & Microsyst. Lab., Tech. Univ. Dresden, Germany
Publication Date: Proceedings of 3rd International Conference on Adhesive Joining and Coating Technology in Electronics Manufacturing 1998 (Cat. No.98EX180) p.112-15
Editor(s): Constable, J.H.
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA xii+368 pp.
ISBN: 0 7803 4934 2 Material Identity Number: XX-1998-03270
U.S. Copyright Clearance Center Code: 0 7803 4934 2/98/$10.00
Publication Date: Proceedings of 3rd International Conference on Adhesive Joining and Coating Technology in Electronics Manufacturing 1998. Presented at Adhesives '98
Conference Sponsor: IEEE Components, Packaging & Manuf. Technol. Soc.; Binghamton CPMT Chapter; Integrated Electron. Eng. Center (IEEC); State Univ. New York at Binghamton
Conference Date: 28-30 Sept. 1998 Conference Location: Binghamton, NY,
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P); Experimental (X)
Abstract: Chip size packaging (CSP) is a promising approach in packaging and interconnect technologies in order to solve the increasing demands in microelectronics and microsystems. The application of bare dies to produce electrical components is considered as the major advantage of this packaging concept. In this study, an interposer consisting of a **polyimide** film is attached by a pre-deposited adhesive at the active side of the chip. Photolithography for patterning the conductor lines in a semiadditive processing sequence was employed. Bond wire techniques were used to connect the bond pads at the interposer and the die. The detailed description of the technology focuses on the adhesive deposition, the fabrication of the conductor pattern and the attachment of the pre-fabricated assembly to the board by soldering techniques. (4 Refs)

33/9/14
DIALOG(R) File 2: INSPEC

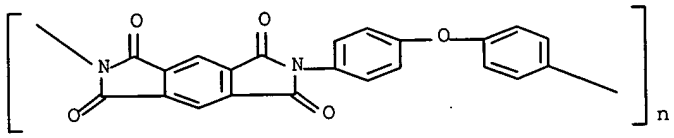
6075367 INSPEC Abstract Number: B9812-0170J-050
Title: Technical evaluation of a near chip scale size **flip chip/plastic ball grid array** package
Author(s): Jimarez, M.; Li Li; Tytran, C.; Loveland, C.; Obrzut, J.
Author Affiliation: Div.. of Microelectron., IBM Corp., Endicott, NY, USA
Conference Title: 1998 Proceedings. 48th Electronic Components and Technology Conference (Cat. No.98CH36206) p.495-502
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA xxv+1476 pp.
ISBN: 0 7803 4526 6 Material Identity Number: XX98-01334
U.S. Copyright Clearance Center Code: 0 7803 4526 6/98/$10.00
Conference Title: 1998 Proceedings. 48th Electronic Components and Technology Conference (Cat. No.98CH36206)
Conference Sponsor: IEEE Components, Packaging & Manuf. Technol. Soc.; Electron. Ind. Assoc
Conference Date: 25-28 May 1998 Conference Location: Seattle, WA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: Technical evaluation and reliability assessment have been performed for a near chip scale size package that utilizes microvias and the **Flip Chip-Plastic Ball Grid Array** technology. The microvias were photolithographically patterned in a build-up, Surface Laminar Circuit/sup TM/ (SLC) **interposer layers** . The package accommodated a 12 mm*14 mm die with 700 controlled collapse chip connections (C4). The carrier dimensions were 21 mm*21 mm, 1.27 mm **pitch** with 255 EGA interconnections. The dimensions of the package, for which the target application was microprocessors, conformed to the JEDEC standards. It has been determined that this novel packaging construction is manufacturable and can satisfy the standard reliability requirements. (7 Refs)

L28 ANSWER 1 OF 2 **HCAPLUS COPYRIGHT ACS on STN**
AN 2003:817845 HCAPLUS Full-text
DN 139:300252
ED Entered STN: 17 Oct 2003
TI **Dielectric interposer** for chip to substrate soldering
IN Brofman, Peter J.; Farooq, Shaji; Knickerbocker, John U.; Langenthal, Scott I.; Ray, Sudipta K.; Stalter, Kathleen A.
PA International Business Machines Corporation, USA
IC ICM **H01L023-48**

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003193093	A1	20031016	US 2003-427459	20030501
	US 6657313	B1	20031202	US 1999-233385	19990119
PRAI	**US 1999-233385**	**A3**	**19990119**		

AB A method of and device for preventing short circuits between solder joints in **flip chip** packaging. The dielec. interposer of the present invention has a plurality of apertures or vias which correspond to the I/O pads on a chip and substrate. Preferably, the **interposer** comprises a polyester film, glass, alumina, **polyimide**, a heat curable polymer or an inorg. powder filler in an organic material. More preferably, the interposer contains an adhesive or has adhesive layers disposed on the linear surfaces of the interposer. Cone shaped solder elements are formed within the apertures of the interposer. The dielec. interposer is positioned between a chip and substrate in an electronic module and thermally re-flowed to create an elec. and mech. interconnection. The interposer prohibits contact between the solder joints by isolating each of the joints and corresponding bonding pads. The interposer also prevents over compression of the solder joints by acting as a stand off.

IT Electric insulators
(**interposer**; dielec. **interposer** for chip to substrate soldering)
IT **25036-53-7, Kapton**
(dielec. **interposer** for chip to substrate soldering)
RN 25036-53-7 HCAPLUS
CN Poly[(5,7-dihydro-1,3,5,7-tetraoxobenzo[1,2-c:4,5-c']dipyrrole-2,6(1H,3H)-diyl)-1,4-phenyleneoxy-1,4-phenylene] (9CI) (CA INDEX NAME)



L41 **ANSWER 8 OF 8 HCAPLUS COPYRIGHT ACS on STN**

AN 1998:684925 HCAPLUS Full-text

DN 129:303473

ED Entered STN: 29 Oct 1998

TI Circuit connecting materials, and structure and method of connecting circuit terminal

IN Watanabe, Itsuo; Fujinawa, Touru; Arifuku, Motohiro; Kanazawa, Houko; Kuwano, Atsusi

PA Hitachi Chemical Co., Ltd., Japan

IC ICM C09J201-00
ICS C09J009-02; C09J161-00; C09J163-00; C08L101-00; C08L061-00; C08L063-00; C08K005-14; H01B001-20; **H01L021-60**

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	**WO 9844067**	**A1**	**19981008**	**WO 1998-JP1467**	**19980331**
	AU 9865207	**A1**	**19981022**	**AU 1998-65207**	**19980331**
	EP 979854	**A1**	**20000216**	**EP 1998-911125**	**19980331**
	JP 2004128465	A2	20040422	JP 2003-186397	20030630
PRAI	JP 1997-79422	A	19970331		
	JP 1997-79424	A	19970331		
	JP 1997-252933	A	19970918		
	JP 1998-541457	A3	19980331		
	WO 1998-JP1467	W	19980331		

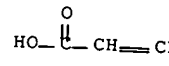
AB The invention concerns a circuit connecting material to be **interposed** between circuit electrodes facing each other and, when the facing electrodes are pressed against each other, to elec. connect the electrodes in the pressing direction, which comprises as the essential ingredients (1) a hardener generating free radicals upon heating, (2) a hydroxylated resin having a mol. weight of 10,000 or higher, and (3) a radical-polymerizable substance; and a structure and method of connecting a circuit terminal by using the material. Mixing a 40 % solution of PKHC (phenoxy resin) in PhMe/vinyl acetate mixture, 50, with Epolite 80MFA 50 and Percure HO (a peroxide) 5 g, combining the mixture with 3 vol% Ni-plated polystyrene particles as elec. conductors, coating on a **80-μm** PET polyester film and drying at 70.degree. for 10 min gave an adhesive film for adhering flexible circuit board.

IT Printed circuit boards
(circuit connecting materials, and structure and method of connecting circuit terminal)

IT **79-10-7D**, 2-Propenoic acid, esters with phosphoric acid and glycol, uses **25068-38-6**, PKHC
(circuit connecting materials, and structure and method of connecting circuit terminal)

RN 79-10-7 HCAPLUS

CN 2-Propenoic acid (9CI) (CA INDEX NAME)

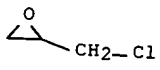


RN 25068-38-6 HCAPLUS

CN Phenol, 4,4'-(1-methylethylidene)bis-, polymer with (chloromethyl)oxirane

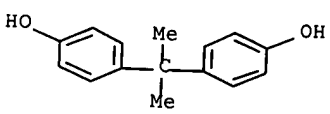
CM 1

CRN 106-89-8
CMF C3 H5 Cl O



CM 2

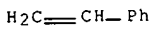
CRN 80-05-7
CMF C15 H16 O2



IT **9003-53-6**, Polystyrene
RL: TEM (Technical or engineered material use); USES (Uses)
(nickel-plated powder, elec. conductors; in circuit connecting materials, and structure and method of connecting circuit terminal)
RN 9003-53-6 HCAPLUS
CN Benzene, ethenyl-, homopolymer (9CI) (CA INDEX NAME)

CM 1

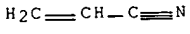
CRN 100-42-5
CMF C8 H8



IT **9003-18-3**
RL: POF (Polymer in formulation); PRP (Properties); TEM (Technical or engineered material use); USES (Uses)
(nitrile rubber, carboxy-terminated, blend, Hycar CTBNX 1009SP; circuit connecting materials, and structure and method of connecting circuit terminal)
RN 9003-18-3 HCAPLUS
CN 2-Propenenitrile, polymer with 1,3-butadiene (9CI) (CA INDEX NAME)

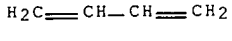
CM 1

CRN 107-13-1
CMF C3 H3 N



CM 2

CRN 106-99-0
CMF C4 H6



36/9/7
DIALOG(R) File 2: INSPEC

5624589 INSPEC Abstract Number: B9708-0170J-058
Title: Development of flip chip BGA
Author(s): Fujita, Y.; Hirakawa, A.; Shibuya, H.; Hattori, S.
Journal: Oki Technical Review vol.63, no.158 p.73-6
Publisher: Oki Electric Industry,
Publication Date: April 1997 Country of Publication: Japan
CODEN: OTREDF ISSN: 0912-5566
SICI: 0912-5566(199704)63:158L.73:DFC;1-0
Material Identity Number: D938-97002
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: We developed a flip chip BGA (**Ball Grid Array**) package. Considering applications to a larger chip, the solder bump of the flip chip connection is made of high temperature solder, which is soft and absorbs stress. For the **interposer, a high heat resistant resin board** was used, since such a board has low cost and can withstand temperatures of the melting point of a high temperature solder bump. To relax the stress generated at the bump and to protect from moisture we optimized the under fill resin, which fills the area between the chip and board. The results of tests confirmed the high reliability of these BGA communications packages with twice or more the target temperature cycles. (3 Refs)

L6 **ANSWER** 12 OF 15 **WPIX COPYRIGHT THOMSON DERWENT on STN**
AN 1997-322497 [30] WPIX Full-text
DNN N1997-266860 DNC C1997-104319
TI Large scale integration semiconductor device - comprises two stacked chips, functional elements electrically connected via bumps formed on electrodes, and **interposed insulating resin.**
DC L03 U11
IN KAWAKIA, T; MATSUMURA, K; YAMANE, I; KAWAKITA, T
PA (MATU) MATSUSHITA ELECTRIC IND CO LTD; (MATE) MATSUSHITA ELECTRONICS CORP; (MATU) MATSUSHITA DENKI SANGYO KK
CYC 6

PI	EP 780893	A2 19970625 (199730)* EN	32	H01L021-66	
	JP 09232379	A 19970905 (199746)	13	H01L021-60	
	US 5734199	**A 19980331 (199820)**	**29**	**H01L023-52**	**<--**
	US 5811351	**A 19980922 (199845)**		**H01L021-44**	
	KR 97053206	A 19970729 (199910)		H01L021-60	

ADT EP 780893 A2 EP 1996-119457 19961204; JP 09232379 A JP 1996-292303 19961105; US 5734199 A US 1996-767778 19961217; US 5811351 A Div ex US 1996-767778 19961217, US 1997-978270 19971125; KR 97053206 A KR 1996-59482 19961129
FDT US 5811351 A Div ex US 5734199
PRAI JP 1995-328519 19951218
IC ICM H01L021-44; H01L021-60; H01L021-66; **H01L023-52**
ICS H01L021-321; H01L023-48; H05K003-34

AB EP 780893 A UPAB: 19970723
A semiconductor device comprises: (i) first and second functional chips (110,120) each having a test electrode (111,121) and a connecting electrode (112,122) of smaller area than the test electrode; (ii) a bump (113,123) on the connecting electrodes; (iii) **interposed insulating resin** (130) integrating the two chips with their main surfaces opposed; and (iv) a connection between the functional element on the first chip and the second chip, via the electrode bump. Also claimed is a manufacturing method for the above device, including forming a bump on the connecting electrode(s), bonding the electrodes via the bump(s), and integrating the two chips via the insulating resin.

USE - Used in high performance LSI for advanced electronic systems, e.g. multimedia or portable system.

ADVANTAGE - A higher degree of miniaturisation is obtained with reliable inter-chip electrical connection. Dwg.1/22

L6 **ANSWER** 14 OF 15 **WPIX COPYRIGHT THOMSON DERWENT on STN**
AN 1995-378202 [49] WPIX Full-text
CR 1989-170725 [23]; 1995-378203 [48]
DNN N1995-278011 DNC C1995-163015
TI Resin sealed semiconductor device - has sealing **resin interposed** between **insulated** top face of lead frame and back side of semiconductor element, etc., giving improved reliability.
DC A85 L03 U11
PA (HITA) HITACHI LTD
CYC 1
PI JP 07254681 A 19951003 (199549)* 5 H01L023-50 <--
ADT JP 07254681 A Div ex JP 1987-270180 19871028, JP 1995-23686 19871028
PRAI JP 1987-270180 19871028; JP 1995-23686 19871028
IC ICM **H01L023-50**
ICS H01L023-28
AB JP 07254681 A UPAB: 19951211
The device has a semiconductor element (1) which is sealed completely and bonded to an internal lead of a lead frame (4). The internal lead is placed at the back side of element. An electrode is placed at both the ends of the upper surface of the element. The connection between the two leads and the two electrodes is made by a wire (3). Since the lead and the element are connected electrically through the electrode, the lead and the element are to be insulated. Hence, one end of each lead of the lead frame is connected to the element through a long tape (7a,7b) which acts as an electric insulator. The other ends of the two leads which is extended upto the centre of the element is insulated by providing a second electric insulator (12). A gap is generated between the element and the second insulator. A sealing resin is used to fill the gap between the second insulator and the backside of the element.
ADVANTAGE - The reliability of the device is improved. Cracking of the element due to heat is prevented. Dwg.3/6

L6 **ANSWER** 15 OF 15 **WPIX COPYRIGHT THOMSON DERWENT on STN**
AN 1994-179772 [22] WPIX Full-text
DNN N1994-141731 DNC C1994-082070
TI Electronic parts mounting board mfr. - by mounting resin sealing frame on **insulating** board while **interposing** semi-hardened **epoxy resin**, heating and applying pressure.
DC A85 L03 U11 V04
PA (IBIG) IBIDEN CO LTD
CYC 1
PI JP 06120373 A 19940428 (199422)* 7 H01L023-14 <--
ADT JP 06120373 A JP 1992-289527 19921002
PRAI JP 1992-289527 19921002
IC ICM **H01L023-14**
ICS H01L023-28

L6 **ANSWER** 13 OF 15 **WPIX COPYRIGHT THOMSON DERWENT on STN**
AN 1996-326943 [33] WPIX Full-text
DNN N1996-275452 DNC C1996-103723
TI Electronic component mounting type lead frame - has **insulating resin interposed** between under surface of electric component and upper face of mounting surface.
DC A85 L03 U11 V04
PA (DENK) TDK CORP
CYC 1
PI JP 08148636 A 19960607 (199633)* 7 H01L023-50 <--
ADT JP 08148636 A JP 1994-285713 19941118
PRAI JP 1994-285713 19941118
IC ICM **H01L023-50**
ICS H05K007-04
AB JP 08148636 A UPAB: 19960823
The lead frame consists of a land part (5) which is soldered to the terminal of an electric component (1), mounted on an electric component mounting surface.

An **insulating resin** is made to **interpose** between the under surface of the electric component and the upper face of the mounting surface.

ADVANTAGE - Maintains insulation resistance between electric component and lead frame. Improves insulated breakdown voltage. Dwg.1/16

36/9/8
DIALOG(R) File 2: INSPEC

4828915 INSPEC Abstract Number: B9501-0170J-011, C9501-5490-003
Title: Area array interconnection with Cu-PI thin films on a multi-layer glass-ceramic substrate
Author(s): Howell, W.J.; Ference, T.G.; Rao, V.; Scheid, D.; Budnaitis, J.; Streif, R.
Author Affiliation: IBM Corp., Hopewell Junction, NY, USA
p.579-83
Publisher: IEEE, New York, NY, USA
Publication Date: 1993 Country of Publication: USA xvii+1166 pp.
ISBN: 0 7803 0794 1
U.S. Copyright Clearance Center Code: 0569-5503/93/0000-0579$3.00
Conference Title: Proceedings of IEEE 43rd Electronic Components and Technology Conference (ECTC '93)
Conference Date: 1-4 June 1993 Conference Location: Orlando, FL, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P)
Abstract: The microelectronic packaging technology for the SS-1 supercomputer utilizes an **interposer** to interconnect integrated circuit devices. Area array solder **bump** interconnection has been used successfully in attaching both chips to the **interposer**, a Cu-**PI thin film** /multi-layer glass-ceramic substrate, and attaching this **interposer** to a larger Cu-**PI** thin film/glass-ceramic substrate. This highly reliable chip interconnection technology has been extended to **interposer** to substrate interconnection, with commensurate increases in both the interconnection density and total number of I/O connections per module. In this paper, key elements of both the **flip-chip** and **interposer** join and replace processes are reviewed. Additionally, optimization of the thin film metallurgy and join/replace parameters necessary to achieve high reliability are presented. (9 Refs)
Descriptors: **flip-chip** devices; integrated circuit interconnections; integrated circuit packaging; integrated circuit reliability; mainframes; multichip modules; **polymer** films; soldering

36/9/9
DIALOG(R) File 2: INSPEC

4823496 INSPEC Abstract Number: B9412-2240-012
Title: Manufacture of advanced Cu-**PI** multi chip modules
Author(s): Rao, V.; Hutchins, D.; Reagan, J.; Scheid, D.; Streif, R.; Syrstad, T.; Eggerding, C.; Redmond, T.
Author Affiliation: IBM Corp., East Fishkill, NY, USA
p.920-34
Publisher: IEEE, New York, NY, USA
Publication Date: 1993 Country of Publication: USA xvii+1166 pp.
ISBN: 0 7803 0794 1
U.S. Copyright Clearance Center Code: 0569-5503/93/0000-0920$05.60
Conference Title: Proceedings of IEEE 43rd Electronic Components and Technology Conference (ECTC '93)
Conference Date: 1-4 June 1993 Conference Location: Orlando, FL, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: A process has been developed for fabricating advanced Cu-PI multi chip modules (MCMs). This technology has been in prototype manufacturing for three years. Several thousand MCM's or **interposers**, with exceptional AC and DC characteristics, have been manufactured and used in prototype systems. Each **interposer** allows interconnection for 4 integrated circuits, 18 chip resistors, and 9 decoupling chip capacitors. Components are attached to the **interposer** by a **flip-chip** (or C4) process. The **interposers** are in turn attached to larger substrates. **Interposers** are made up of multilayer thin film (MLTF) on a multilayer glass ceramic substrate. The MLTF consists of 7 metal layers (4 wiring, 3 power-ground). An **interposer** measures less than 25 mm on a side. For four signal **layers**, the **interposer** provides as much as 500 cm/cm/sup 2/ or roughly 20 meters of wiring. There are several thousand signal and power vias in each **interposer**, for a total via density in excess of 800 vias/cm/sup 2/. The physical and electrical characteristics of the **interposers** , the process and test details, manufacturing information, and reliability data are presented. (3 Refs)
Descriptors: circuit reliability; copper; integrated circuit manufacture; integrated circuit testing; microassembling; multichip modules; **polymer** films; production testing; substrates; surface mount technology; thin film circuits

L34 ANSWER 2 OF 2 **HCAPLUS COPYRIGHT ACS on STN**
AN 1982:440074 HCAPLUS Full-text
DN 97:40074
ED Entered STN: 12 May 1984
TI Laminates
IN Miyadera, Yasuo; Fujioka, Atsushi; Kumazawa, Tetsuo; Doi, Hiroaki
PA Hitachi Chemical Co., Ltd., Japan; Hitachi, Ltd.

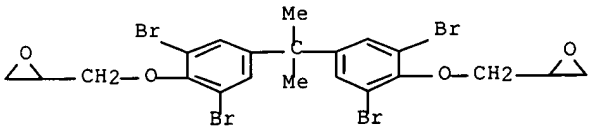
	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	**EP 50855**	**A1**	**19820505**	**EP 1981-108775**	**19811023**
	EP 50855	**B1**	**19841219**		
	JP 57072847	A2	19820507	JP 1980-149459	19801027
	JP 57074149	A2	19820510	JP 1980-149460	19801027
	JP 01047299	B4	19891013		
	JP 57074150	A2	19820510	JP 1980-149463	19801027
	JP 01007863	B4	19890210		
PRAI	JP 1980-149459		19801027		
	JP 1980-149460		19801027		
	JP 1980-149463		19801027		

AB Laminates prepared by molding under heat and pressure prepregs of resin-impregnated composite fabrics (woven or nonwoven) comprising aromatic polyamide fibers and glass fibers have a low linear expansion coefficient and excellent interlaminar strength. Thus, prepregs were prepared by dipping a composite cloth of glass fibers and Kevlar 49 fibers in a varnish comprising Araldite 8011 (brominated bisphenol A type epoxy resin) [**67383-03-3**] 90, ECN 1280 (cresol novolak type epoxy resin) [63992-68-7] 10, dicyandiamide 4, and benzyldimethylamine 0.2 part dissolved in MEK and Me Cellosolve to give a 37% resin content and drying at 160° for 5 min. Eight plys of these prepregs were **interposed** between 2 Cu foils (35 μ thick) and pressed 60 min at 170° to give a 1.03 mm-thick laminate. The linear expansion coefficient of the laminate in the plane direction was 5.8 + 10-6/°C. The peel strength of the Cu foil was 1.9 kg/cm, and th interlaminar strength was ≥2.5 kg/cm.

IT Epoxy resins, uses and miscellaneous
(laminates with copper, glass fibers and polyamide fibers, having low linear expansion coefficient and high interlaminar strength)
IT **33294-14-3**
(blends with epoxy resins, laminates with copper, glass fibers and polyamide fibers, having low linear expansion coefficient and high interlaminar strength)
RN 33294-14-3 HCAPLUS
CN Oxirane, 2,2'-[(1-methylethylidene)bis[(2,6-dibromo-4,1-phenylene)oxymethylene]]bis-, homopolymer
CM 1

FR 4

CRN 3072-84-2
CMF C21 H20 Br4 O4



PACKAGING RELIABILITY, CHIP-SCALE SEMICONDUCTOR

Pradeep Lall, Motorola, Inc.

J. Webster (ed.), *Wiley Encyclopedia of Electrical and Electronics Engineering Online*

Article Online Posting Date: December 27, 1999

PACKAGE ARCHITECTURE - AN OVERVIEW

Flex-Substrate Ball-Grid Array Packages

The flex-substrate BGA is a chip-scale package that consists of a chip wirebonded to a single-sided flex-polyimide substrate (75 μm thick). The wirebonded assembly is overmolded. All the package inputs and outputs (I/Os) that communicate with the board are routed to pads on the chip side of the polyimide substrate. The package-to-board connections are made with 63% Sn-37% Pb solder balls, which go through holes in the substrate and connect to the solder pads on the chip side of the polyimide substrate (Fig. 1). The flex-substrate BGA has 0.45 mm solder balls at 0.8 mm pitch.

Elastomer-on-Flex Packages

The elastomer-on-flex package is a BGA format chip-scale package. The package consists of a chip flipped onto an elastomeric substrate. All the I/Os of the chip are routed to a single-sided flexible circuit, which is bonded to the other side of the elastomeric substrate by beam leads (gold, 18 μm thick). The beam leads are extensions of the printed circuit on the flexible circuit, which are connected to 63% Sn-37% Pb solder balls. The package is exactly the size of the chip, is 80% smaller than a comparable 40-lead thin-small outline package (TSOP) and is 17% thinner, measuring just 1 mm in thickness. The elastomer-on-flex 48-I/O package has 0.3 mm (11.81 mil) diameter solder balls at 0.65 mm pitch (Fig. 2). Two versions of the elastomer-on-flex interposer CSP (from a single source) have been characterized in this study - the 48-pin and the 40-pin. Both the 40-bump and 48-bump versions have 0.3 mm (11.81 mils) diameter solder balls at 0.75 mm pitch (Figs. 2 to 5[fig 2, fig 3, fig 4, fig 5]).

Rigid-Interposer Flip-Chip Packages

Figure 6 is a schematic of a Motorola SLICC (or Motorola JACS-Pak) package mounted to a main printed circuit board (PCB); Table 1 gives typical characteristics. An IC with high-lead solder bumps (e.g., 97% Pb-3% Sn or 95% Pb-5% Sn) is reflowed to a BT-epoxy (Bismaleimide Triazine) PCB interposer substrate 0.2 mm to 0.3 mm (8 to 12 mils) thick and underfilled using conventional flip-chip processes. Active I/Os are routed, through PTHs (plated-thru hole), to an array of solder pads on the underside of the package, as in pad array carriers such as the plastic ball-grid array (PBGA) package (Figs. 6, 7). The SLICC bottom-side package solder-joint pad pitch is 32 mils (0.8 mm). These pads are bumped with solder spheres of 22.2 mil (0.564 mm) diameter. SLICC packaging has extended the existing pad array carrier technology limits both in pad-pitch and in solder-sphere size. SLICCs for ICs with I/O counts in the range from 40 to 150 can be made about 0.060 in. to 0.100 in. (0.15 cm to 0.25 cm) larger than the IC on a side. The area efficiency is greatly enhanced for the SLICC package over wirebonded packages [OMPAC, Quad-Flat Package (QFP) etc.] because of the increased area that is available to route the runners under the IC. This area underneath the IC is critical to routing the I/Os from the IC to the bottom side in the most efficient manner. As PCB technologies lend themselves to finer lines and spaces, smaller plated vias, and better tolerances, this approach can result in carriers that can theoretically be the same size as the IC in the x and y dimensions.

The flip chip is assembled to the interposer board via alignment on the C4 bump cell and subsequent reflow soldering in a convection reflow process. The low-temperature solder on the board reflows and

forms the interconnect between the chip and the board. The high-temperature solder on the chip is not reflowed, and the presence of this solder bump helps maintain the standoff between the chip and the board. The C4 bonded chip is then underfilled. The package solder-joint bumping is done using the conventional BGA bumping process.

Chip bonding consists of four substeps: (a) chip alignment, (b) flux dispense, (c) chip placement, (d) reflow. Prior to any processing, the interposer substrate is fixtured into a specially designed pallet to prevent substrate warpage after chip placement. The chips are flipped face down in the waffle packs prior to mounting the waffle packs for chip placement. The chips are picked from the waffle packs and visually aligned (using the imaging system on the C4 bump cell) so that the pads on the interposer substrate overlap the bumps on the chip. Flux is then dispensed at the bonding site on the interposer substrate. The chip is placed immediately after dispense, before the flux dries up. This is very important, since the flux contains a tacky medium that holds the chip in place during population of the interposer substrate and transfer to the convection furnace, and in the convection furnace prior to reflow. After the chips have been placed on the interposer substrate, the pallet is fed into the reflow oven to form the C4 joints. The low-temperature solder on the interposer wicks up and forms a joint with the high-temperature solder on the chip.

Underfilling is carried out by dispensing underfill material around all of the chip and the material is pulled in by subjecting the assembly to cyclic application of vacuum and air pressure for two or three cycles. Acoustic microscopy has been used to verify the complete underfilling of the chip by vacuum infiltration (Fig. 8). For the underfill to be effective at all, it is extremely important for the material to engulf the solder joints and have maximum adhesion in the peripheral region. The risk to the integrity of the device with some trapped voids in the center is minimal.

The BGA ball-bumping process involves dispensing flux on each of the C5 pads and placing solder spheres. After the array has been populated with solder spheres, it is then reflowed. The array is then singulated by sawing, using precision sawing equipment.

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Figure 6.
Schematic of a SLICC package.

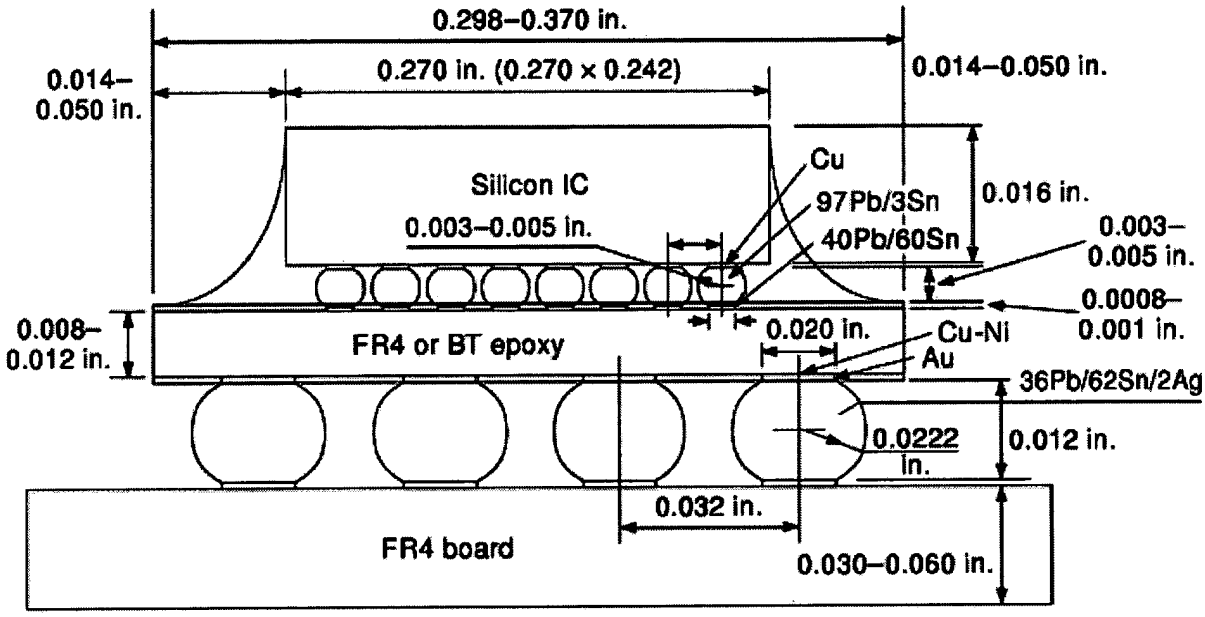

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Table 1. SLICC Characteristics

Size of carrier (in.)	0.028–0.100 larger than IC edge
Thickness of substrate (in.)	0.008–0.012
Substrate materials	FR4, BT-Epoxy
Thickness of topside solder mask (in.)	0.0008–0.001
Height of topside pad finish	0.0008–0.0015
PTH metal	0.0005-in.-thick Cu (typical), plugged
Minimum line widths/spacings (in.)	0.004/0.004
Bottom-side pad finish	Au flash over Cu–Ni
Bottom-side pad pitch[a] (in.)	0.032
Bottom-side pad diameter (in.)	0.020
Bottom-side ball diameter (in.)	0.0222

[a] Center to center.

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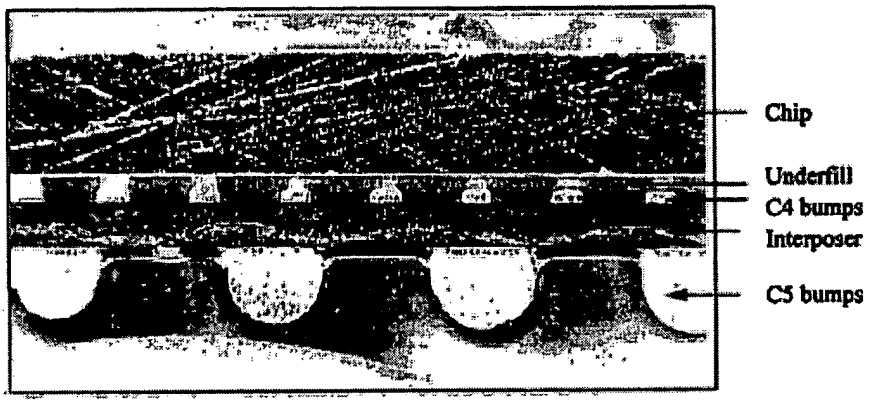
Figure 7.
Cross section of SLICC (JACS-Pak) package.



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Unlike the traditional flexible interposer using thin polyimide film and TAB-like interconnection (Tessera's µBGA®) that use traditional via creation techniques such as laser, plasma, and other mechanical drilling has the following structure:

- http://www.aitechnology.com/sc25.html
  - Image: http://www.aitechnology.com/gbbbck.gif
  - Image: http://www.aitechnology.com/gbhome.gif

Location: http://www.aitechnology.com/sc25.html
File MIME Type: text/html
Source: Currently in memory cache
Local cache file: none
Last Modified: Monday, May 22, 2000 11:37:30 PM Local time
Last Modified: Tuesday, May 23, 2000 3:37:30 AM GMT
Content Length: 4254
Expires: No date given
Charset: windows-1252
Security: This is an insecure document that is not encrypted and offers no security protection.

Unlike the traditional flexible interposer using thin polyimide film and TAB-like interconnection (Tessera's µBGA®) that use traditional via creation techniques such as laser, plasma, and other mechanical drilling. The molecularly flexible interposer is much easier to fabricate with both vias and lead routing with the use of dielectric that polymerized into designed matrix of conductor-vias. The cost per lead of this patent pending form-in-place method of interconnection between dielectric surfaces is estimated to be lower than $0.05 for larger volume. Even for the relative lower quantity, the cost per lead is well within $0.10.

CHIP-COUPLER™ technology eliminates the need and problems of using underfills both at the component and board levels. Overall cost of usage of comparable interposers of the same interconnection density cost 2-3 times more than the solution provided with this intrinsically flexible substrate having low dielectric constant and dissipation. Besides using CHIP-COUPLER™ interposer for the construction of fine-pitch components, logistic may be worked out that good parts may be directly soldered onto the proper CHIP-COUPLER™ interposer for final component construction.

CHIP-COUPLER™ technology uses flexible dielectric that has dielectric constant of 3.8 and dissipation of less than 0.01. The modulus of elasticity is 20,000 psi with elongation of more than 100% and glass transition at -55° C. The adhesion to copper is more than 3000 psi with no change in bonding after 85°C/85%RH aging. The thermal stability is high and demonstrating a thermogravimetric degradation temperature of higher than 425°C to allow multiple soldering operations with non-lead or lead solders. Conductor pitch of 10 mil or more can be produced easily with thickness of dielectric 3 mil or thicker. The thickness of dielectric may be as thick as 60% of the pitch.

The usage data of CHIP-COUPLER™ interposers are currently being developed. The standard bonding characteristics for bonding strength and reliability onto copper traces and vias have been tested for under normal 85°C/85%RH, Pressure-Cooker moisture exposure, and 150°C for 1000 hour heat aging. All of these stress conditions caused no change in bond strength within experimental error. Similarly, thermal cycling and shock testings from -65°C to 150°C for the flexible dielectric bonding silicon directly onto copper and aluminum plates all proved to be stable for mechanical bond strength as well as thermal and electrical contact resistance.

The characteristic of flexible dielectric, when specialized metallization is incorporated in these CHIP-COUPLER™ interposers, it may be used as testing membrane for testing electrical interconnection or burn-in testing with standard sockets or connectors.

Dr. Kevin Chung graduated with Physics and Material Sciences degrees from Rutgers University and worked at David Sarnoff Research Center from 1980-1985. He is the founder and CEO of AI Technology, Inc.

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